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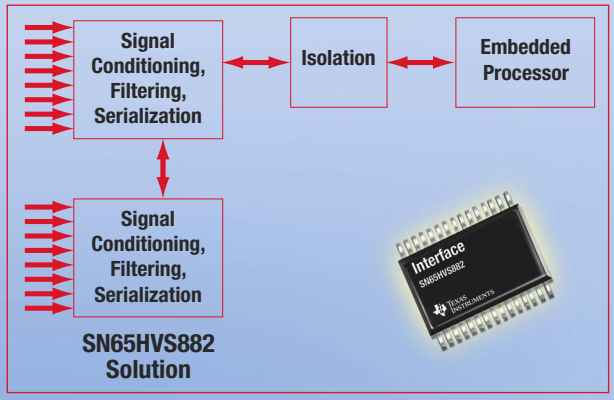

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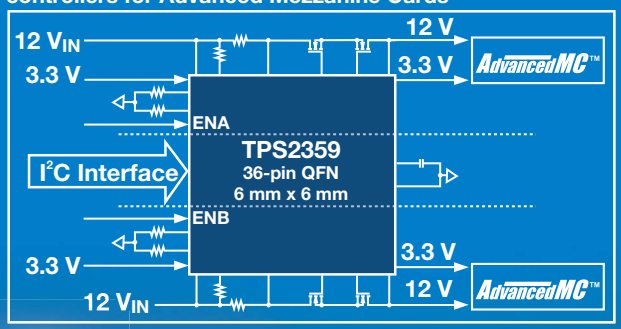

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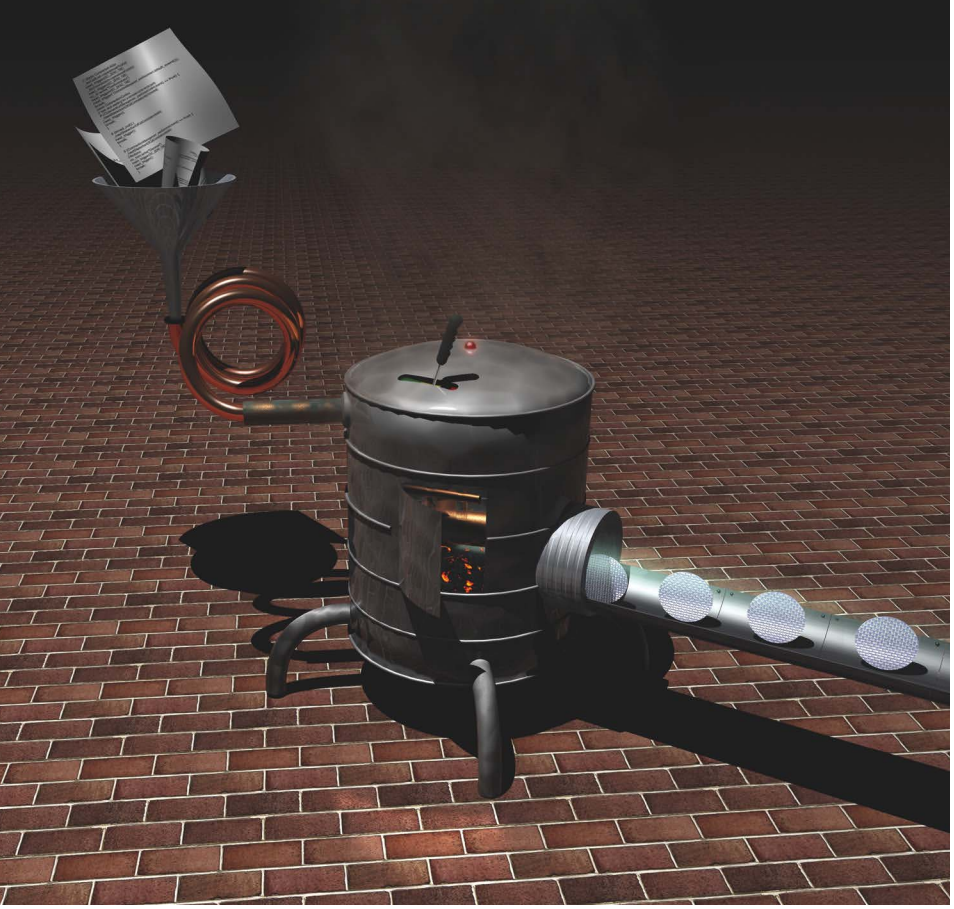

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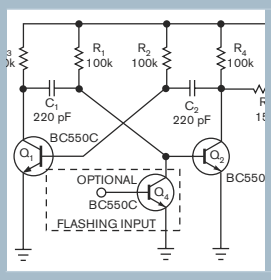

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Leila Ziai,
Staff Design Engineer,
Toshiba America Electronic Components, Inc.

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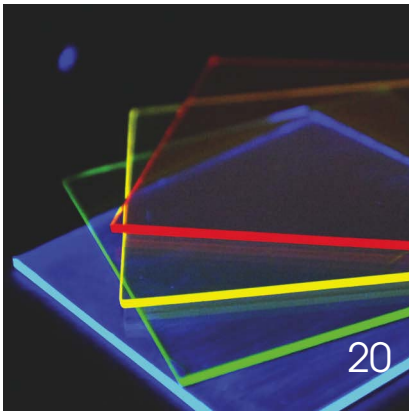
pulse

Dilbert 16



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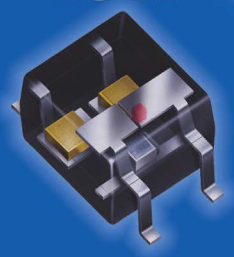

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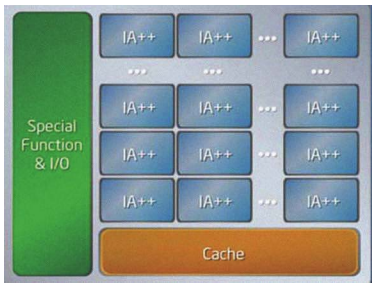

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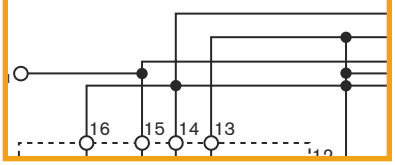

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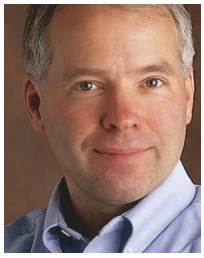

BY RICK NELSON, EDITOR-IN-CHIEF

Hang up and drive; hang up and walk

The cell-phone market is potentially huge. Sanjay K Jha, then chief operating officer of Qualcomm and president of Qualcomm CDMA Technology, said in a June 11 Design Automation Conference keynote address that 2 billion people are wireless subscribers today and that, by 2020, 9 billion people will become potential customers. (Motorola has subsequently hired Jha to serve as co-chief executive officer.) Jha cited one downside to this exploding market: Many of these 9 billion potential subscribers won't spend more than $15 or $20 for their handsets. There is another: Many of these 9 billion will be talking while driving or texting while walking, creating mayhem on the roads and sidewalks.

The growing cell-phone-related mayhem has already drawn attention of legislatures in the United States, and, on July 1, laws banning the use of handheld phones while driving went into effect in California and Washington, complementing laws already in effect in Connecticut, the District of Columbia, New Jersey, New York, and Utah.

Don't get me wrong. I think people talking while driving can be a menace. Unfortunately, however, the laws taking effect don't address the real problem.

The online magazine *Salon* (www.salon.com) recently covered this phenomenon (**Reference 1**). "For years, psychologists who study driving and attention have argued that switching to 'hands free' is not a real solution to the hazards caused by yakking on the mobile in the car," the author, Katharine Mieszkowski, states. She quotes David Strayer, professor of psychology at the University of Utah: "The impairments aren't because your hands aren't on the wheel. It's because your mind isn't on the road"—a contention backed up by magnetic-resonance-imaging experiments that show that conversations distract parts of the brain involved in driving.

A company has been outfitting lampposts in London's East End with padded bumpers to reduce injuries to ambulatory texters.

Mieszkowski also notes that talking on a cell phone while driving is more dangerous than talking with in-car passengers. Passengers, she writes, modulate their conversation in accordance to road conditions, having their own safety in mind. In addition, she quotes Paul Atchley, professor of psychology at the University of Kansas: "Cell-phone conversations are more intense than in-car conversation." Cell-phone conversations have more words per minute, and a driver who stops conversing to deal with traffic will be accosted at exactly the wrong time with "Hey, are you still there?"

I would assume that laws mandating hands-free cell-phone operation would inherently outlaw texting while driving, and that's a good thing. It turns out, however, that many texting-related accidents don't involve texting while driving. In another recent article (**Reference 2**), author Dionne Searcey writes: "A growing group of multitaskers are texting on the go ... while ambulatory. They obliviously ram into walls and doorways or fall down stairs. Out on the streets, they bump into lampposts, parked cars, garbage cans, and other stationary objects."

So what's the solution? Searcey reports that a company has been outfitting lampposts in London's East End with padded bumpers to reduce injuries to ambulatory texters. Well, that's one approach, and it's likely to be more effective than US hands-free-cell-phone laws targeting drivers. For both mobile texters and mobile talkers, however, education, not legislation, would seem to be the more promising road to take. **EDN**

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1. Mieszkowski, Katharine, "Hang up and drive," *Salon*, July 25, 2008, www.salon.com/news/feature/2008/07/25/cell_phone_driving/index.html.
2. Searcey, Dionne, "Generation Text: Emailing on the Go Sends Some Users Into Harm's Way," *The Wall Street Journal*, July 25, 2008, www.wsj.com.

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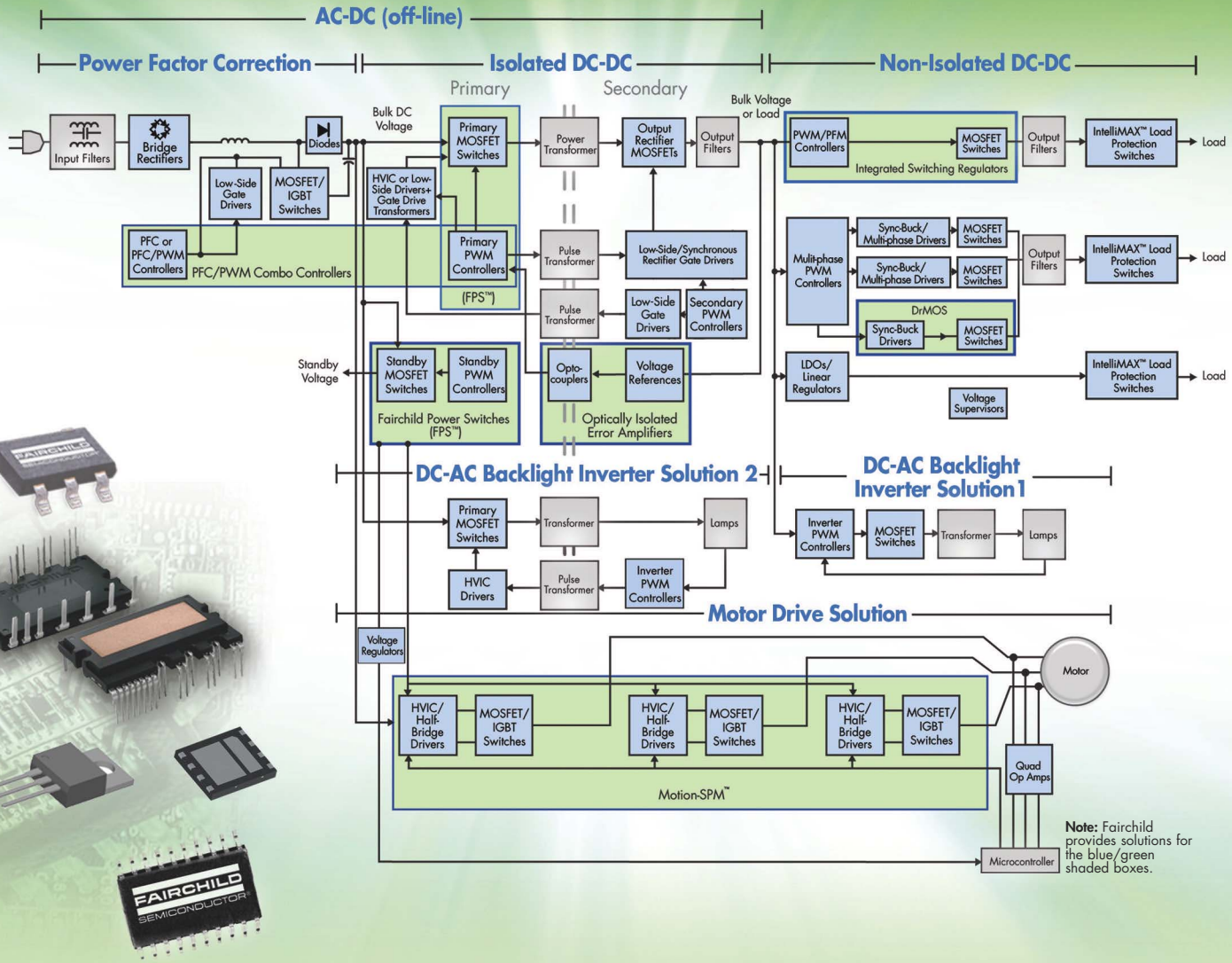

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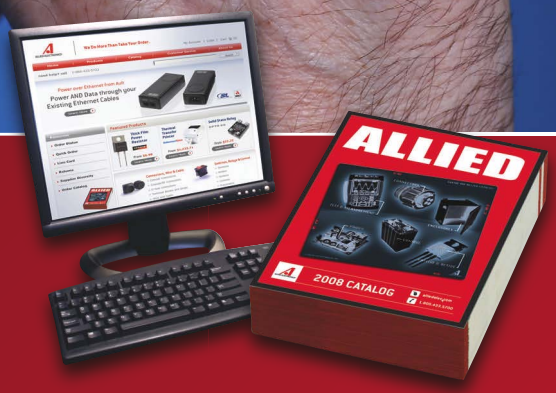

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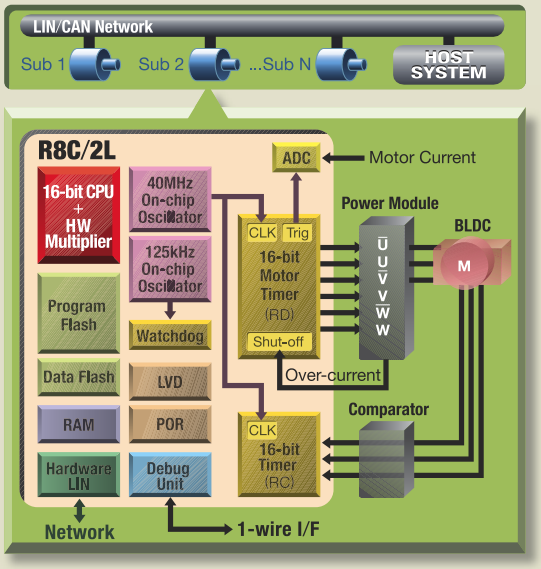

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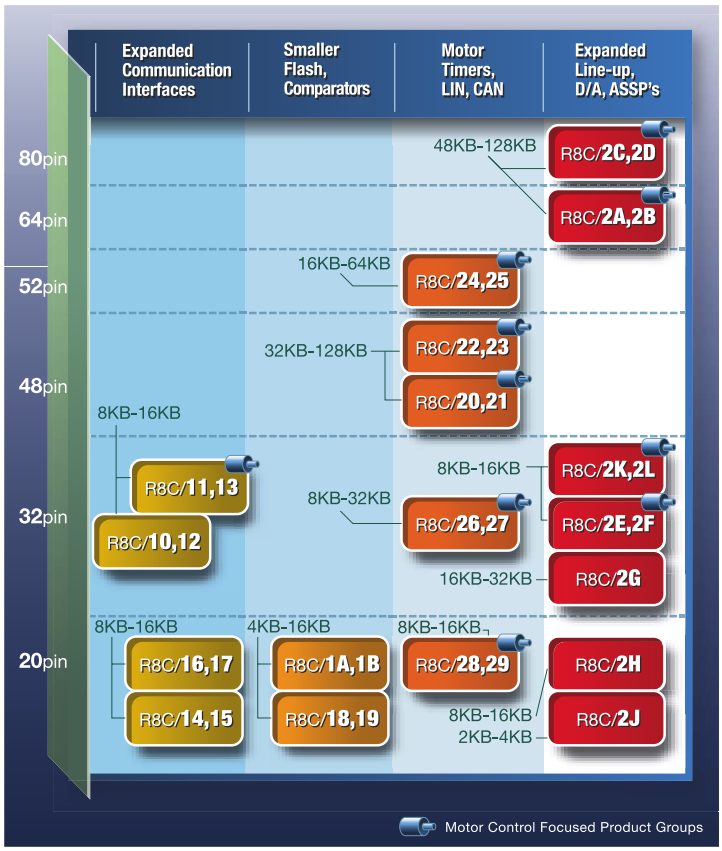

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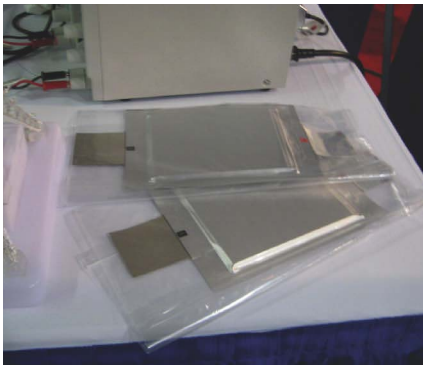


This lithium-ion capacitor measures approximately 5×8 in. and has 1100F capacitance.

JM Energy has now come up with an approach that combines the best features and omits the flaws of both these technologies. The company, an offshoot of petrochemical company JSR Corp (www.jsr.co.jp), has announced a lithium-ion capacitor with energy density of 21to 25 Whr/l, self-discharge of less than 5% after three months, and less than a 10% drop in capacity from initial charge after 100,000 cycles. The units' voltage ranges from 2.2 to 3.8V. The 1000F series has a capacitance of 1100F and an internal dc resistance of 2.5 mΩ; the 2000F series has 2200F capacitance and an internal dc resistance of 1.4 mΩ. JM Energy plans to offer the devices for approximately 10 cents per farad.**—by Margery Conner**

▷**JM Energy**, www.jmenergy.co.jp/en.

FEEDBACK LOOP

"The old Army phrase 'screw up and go up' is the normal situation. I've seen and been associated with some great and talented managers, but they're few and far between. Most are incompetent, lazy egomaniacs playing a political game with their upper managers so they get noticed and jump to the next pay scale."

—Reader William Tell, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6578140. Add your comments.

FPGA IP completes wireless-backhaul method

Wintegra's third-generation UFE3 (universal-front-end-3) IP (intellectual-property) core for high-channel-density, wireless-backhaul designs provides an upgrade path for designers migrating voice-centric cellular systems to high-capacity data-plus-voice-capable designs. The core works with the company's WinPath2 processor and PMC-Sierra's Temux family of framers and mappers. The IP core plus Wintegra's WinPath2 processors at the central office provide bidirectional conversion of 8064 legacy DS0 channels to GbE (gigabit Ethernet), with carrier Ethernet as the link to remote cell sites. The core enables a fully channelized application running any protocol from a list that includes PWE3 (pseudowire end-to-end emulation), MC/ML-PPP (multiclass/multilink point-to-point protocol), IMA (inverse multiplexing over asynchronous transfer mode), and MFR (multilink-frame relay).

A typical example that Wintegra quotes takes an OC (optical-carrier)-12 channel—plus a reserve duplicate channel—from the telecom network and connects it to the PMC-Sierra chip, which interfaces directly to an Altera (www.altera.com) Stratix II FPGA, on which the IP resides. The programmable chip in turn connects to the WinPath2, which bridges the signal to the backplane.

Wintegra supplies the UFE3 soft core for a per-project fee in source code. A reference board from Wintegra features Altera's Stratix II FPGA and PMC-Sierra's Temux 336.

—by Graham Prophet

▷**Wintegra**, www.wintegra.com.

▷**PMC-Sierra**, www.pmc-sierra.com.

Keithley debuts software upgrade and switch/multimeter options

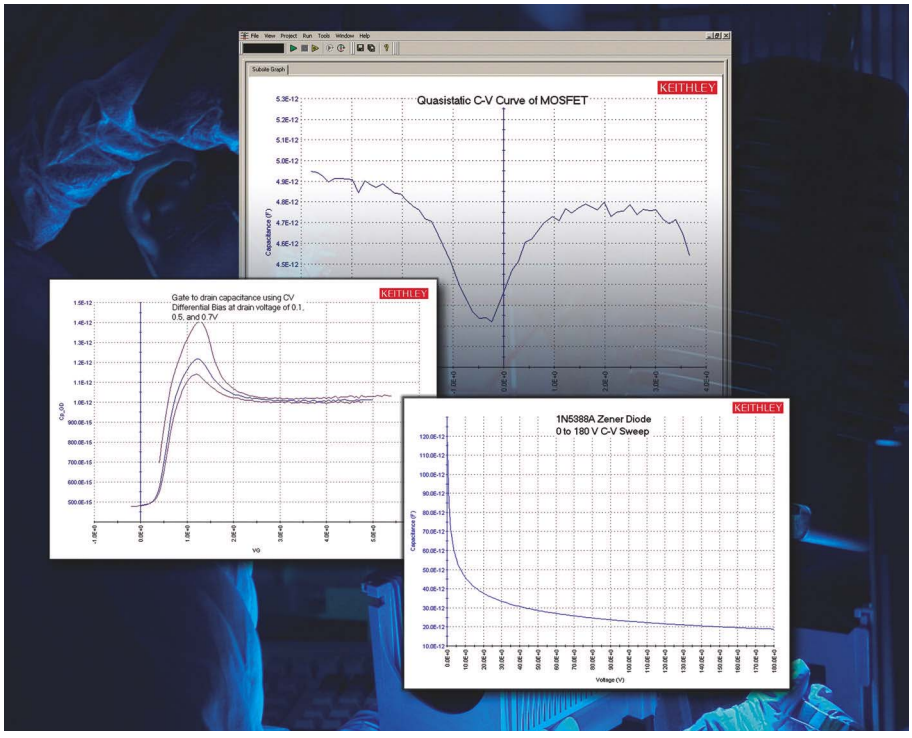
Keithley Instruments at Semicon West (www.semiconwest.org), which took place in San Francisco last month, introduced Version 7.1 of the KTEI (Keithley Test Environment Interactive) for the company's Model 4200-SCS semiconductor-characterization system. The company also announced an expansion of its Series 3700 system family.

The KTEI software upgrade broadens the capabilities of the Model 4200-CVU (capacitance-voltage unit), offering software support for characterizing high-power semiconductor devices at voltages as high as 200V dc or 400V differential voltage and currents as high as 300 mA. This capability is useful for engineers working with LDMOS (laterally diffused metal-oxide semiconductor) and other high-power semiconductor devices in automotive, display, MEMS (microelectromechanical-system), and other high-power applications. KTEI Version 7.1 also adds software support for other new functions, including differential-dc bias and quasi-static capacitance/voltage testing. It offers an expanded set of device-test libraries, as well as a variety of software enhancements to speed and simplify testing.

The company added the Model 3724 dual-1X30 solid-state-FET relay-multiplexer card and the Model 3750 multifunction-I/O card to the Series 3700 system switch/multimeter and plug-in-card family. The Model 3724 card features scanning speeds of greater than 1000 channels/sec, including measurement, and switch-only scan rates of greater than 1200 channels/sec. The card also offers 200V, 0.1A switch/carry capacity with offset current of less than 10 nA. You can automatically configure the solid-state relays into either a dual 1×30 or 1×60 multiplexer. The card also features temperature-measurement capability with automatic CJC (cold-junction-compensation) sensors when you use them with the optional screw-terminal accessory.

The Model 3750 multifunction-I/O card features 40 digital-I/O channels with high-current-driver outputs that can sink as much as 300 mA, allowing them to directly drive relays without any interface circuitry. The Model 3750 also features two programmable analog outputs offering both voltage- and current-programmable isolated analog outputs, including 0 to 20 mA, 4 to 20 mA, or ±12V dc. It also comes with four totalizers/counters with 32-bit resolution and has a 1-MHz input rate. The Model 3724 sells for $1595, and the Model 3750 sells for $1250 (one).—**by Rick Nelson**

▷**Keithley Instruments**, www.keithley.com.



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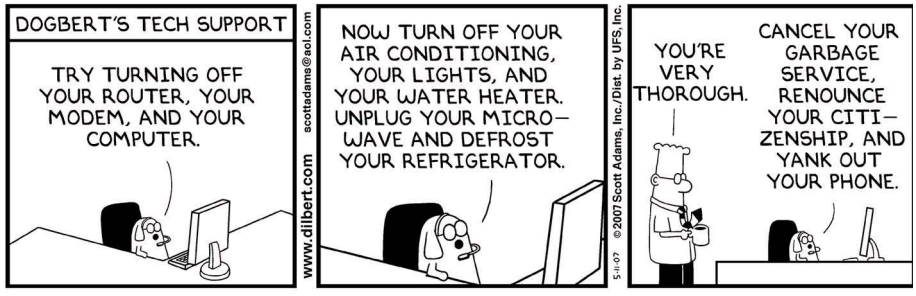
DILBERT By Scott Adams



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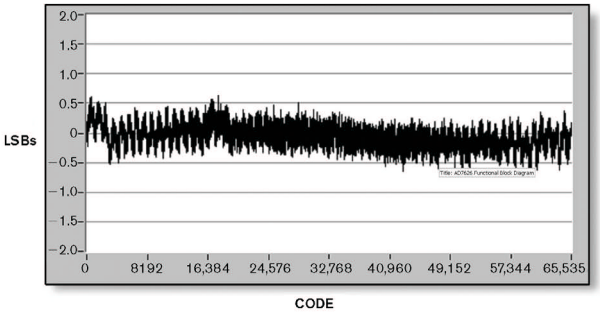
16-bit, 10M-sample/sec ADC uses SAR architecture

Analog Devices' new AD7626 ADC provides 16-bit samples at a 10-MHz rate while using 130 mW. The part targets use in digital-X-ray machines, MRI (magnetic-resonance-imaging) systems, and ATE (automatic-test equipment), as well as general data-acquisition, sonar, and other applications. The differential-input device uses digital-LVDS (low-voltage-differential-signaling) outputs and has an internal 4.096V buffered reference, or you can provide an external reference. A common-mode pin can supply half the reference voltage to the input amplifiers. The device requires both 2.5 and 5V power supplies.



The AD7626 offers an INL of less than 1 bit when it digitizes a 1-kHz input tone at 10M samples/sec.

The AD7626 has good dc performance, with a typical INL (integral nonlinearity) of ±1 bit, as well as no missing codes over its output range. Typical DNL (differential nonlinearity) is ±0.3 bits. The device also offers good ac specs with a 92-dB SNR (signal-to-noise ratio) and an ENOB (effective number of bits) of 15. The part employs a SAR (successive-approximation-register) architecture so that, unlike a pipelined ADC, each clock cycle immediately produces a valid output. Pipelined converters must clock four to six times for the correct conversion data to work its way through the pipeline and appear at the output. This limitation makes pipelined converters less appropriate in multiplexed-system applications, in which the clock-cycle latency creates more software overhead to ensure that the data is valid for a given channel.

The AD7626 is available in a 5×5-mm, 32-pin LFCSP with a suggested retail price of $34 (1000). It operates over a −40 to +85°C temperature range. Production quantities and evaluation modules are available now.**—by Paul Rako**

▷**Analog Devices**, www.analog.com.

08.21.08

MULTIARCHITECTURE-DSP ROAD MAP REFINES POWER-EFFICIENCY-VERSUS-PERFORMANCE BALANCE

Texas Instruments' multiarchitecture-processor plans expand a low-power-design emphasis beyond the fixed-point C550x series of processors and applies it to the high-performance C640x family, the floating-point C674x family, and the high-integration OMAP (Open Multimedia Applications Platform)-L1x family of processors. This shift addresses developers' increasing requests for processing options in different power budgets rather than power consumption for a given level of performance. New devices in each of these product lines will support software and pin-for-pin compatibility so that developers can immediately begin designing with currently available devices and then migrate to devices that consume less power.

The first devices available in this lineup are a new generation of the C674x floating-point DSP family; they will become available for sampling in the fourth quarter of 2008, and prices will start at less than $9 (100). The devices support a deep-sleep power draw of 6 mW using a 0.95V core with the real-time clock on and the DSP and all peripheral clocks off. The power draw is 12 mW in standby mode with the same operating scenario but with the PLL (phase-locked loop) enabled. Active power draw is at 420 mW with an operating scenario using a 1.2V core running at 300 MHz; the McBSP (multichannel buffered serial port), SPI (serial-peripheral interface), and general-purpose I/Os active; and 50% access of the 16-bit mobile DDR at 133 MHz. These numbers represent one-third the power consumption of the previous floating-point devices with a 20-times improvement in standby power.

TI slates the availability of the other next-generation low-power families for 2009. The C640x devices deliver twice the processing performance of the currently available low-power DSPs. The C550x devices halve the low-power operation to 6.8 µW in deep-sleep mode, 0.34 mW in standby mode, and 18 mW in active mode using a 1.05V core running at 60 MHz with 75% DMAC (direct-memory-access-controller) usage and 25% addition operations at normal operating temperature. Active power consumption for a 1.3V core running at 100 MHz with 75% DMAC usage and 25% addition operations at normal operating temperature is 46 mW.

All four of the new processor families emphasize low-power operation.

—by Robert Cravotta

▶**Texas Instruments, www.ti.com.**

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ANALOG DEVICES

RESEARCH UPDATE

BY MATTHEW MILLER AND ANN STEFFORA MUTSCHLER

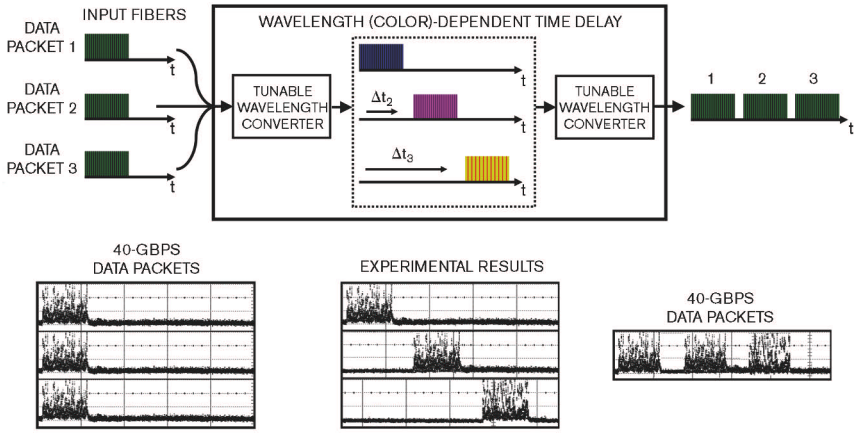
Photonics researchers decelerate light to accelerate data

A research team at the USC (University of Southern California) Viterbi School of Engineering has received $4.3 million in DARPA (Defense Advanced Research Projects Agency) funding to develop continuously tunable optical delays, which could accomplish tasks such as multiplexing entirely in the photonic domain—without the inefficient conversion of light streams into electronic signals and back again.

The work hinges on passing light of a particular "color," or wavelength, through an element that slows that wavelength. By applying a different color-dependent delay to each of multiple photonic data streams, the researchers enable buffering, interleaving, multiplexing, demultiplexing, and synchronization—all without subjecting the speedy streams to the comparative brick wall of an electronic interface. The researchers report that they have successfully delayed an 80-Gbps data stream and multiplexed two 40-Gbps streams. They expect to reach capacity in the hundreds of gigabits per second and aim to produce a system that can delay light by as much as 5 msec, which would represent a 50-fold improvement over the 100-nsec result they have published thus far.

—MM

▷**USC Viterbi**, www.viterbi.usc.edu.



Light-slowing materials permit researchers to introduce wavelength-dependent time delays onto photonic data streams, thus enabling applications such as multiplexing (courtesy USC Viterbi School of Engineering).

Kerf-free wafering technology reduces polysilicon for photovoltaics

To substantially reduce the amount of polysilicon within the ingot-to-wafer manufacturing steps and eliminate some of the costly consumables in today's wafer manufacturing, Silicon Genesis has produced solar substrates for photovoltaic applications using its "kerf-free" wafer-processing technology. The company's PolyMax technology aims to eliminate material losses that occur during sawing; the term *kerf* refers to the width of the cut a saw blade makes. The company says its technology creates high-efficiency solar cells without sawing, grinding, or other mechanical thinning of wafers.

The adoption of the technology could help relax the shortage of polysilicon feedstock, according to Silicon Genesis. The company says it has produced 50-micron-thick, 125-mm wafer samples with excellent mechanical and electrical characteristics. The company plans to start pilot-line operations by spring 2009 to demonstrate kerf-free processing of silicon ingots into wafers ranging from 50 to 150 microns in thickness.

A 125×125-mm, 50-micron PolyMax solar wafer has excellent mechanical and electrical characteristics.

—ASM

▷**Silicon Genesis**, www.sigen.net.

TECHNOLOGY GIVES WINDOWS A SOLAR EDGE

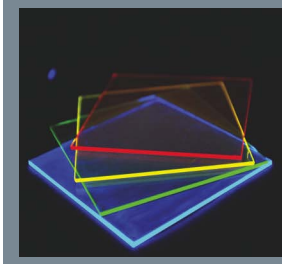
08.21.08

Researchers at the Massachusetts Institute of Technology have developed a technology that transforms a pane of glass into a solar concentrator that can gather light over its entire surface and conduct that light to solar cells along its edges. Employing dyes that trap wavelengths of light inside the pane, the technology can increase the power from solar cells by 40 times, according to the MIT team. Moreover, the technology is simple to manufacture, leading to significant cost savings over current concentrators, which involve mirrors that mechanically track the sun's motion.

A spin-off company, Covalent Solar, hopes to commercialize the technology within three years.—MM

▶Massachusetts Institute of Technology, www.mit.edu.

▶Covalent Solar, www.covalentsolar.com.



A system of organic dyes allows panes of glass to concentrate light for collection by solar cells at the glass' edge (courtesy Donna Coveny, MIT).

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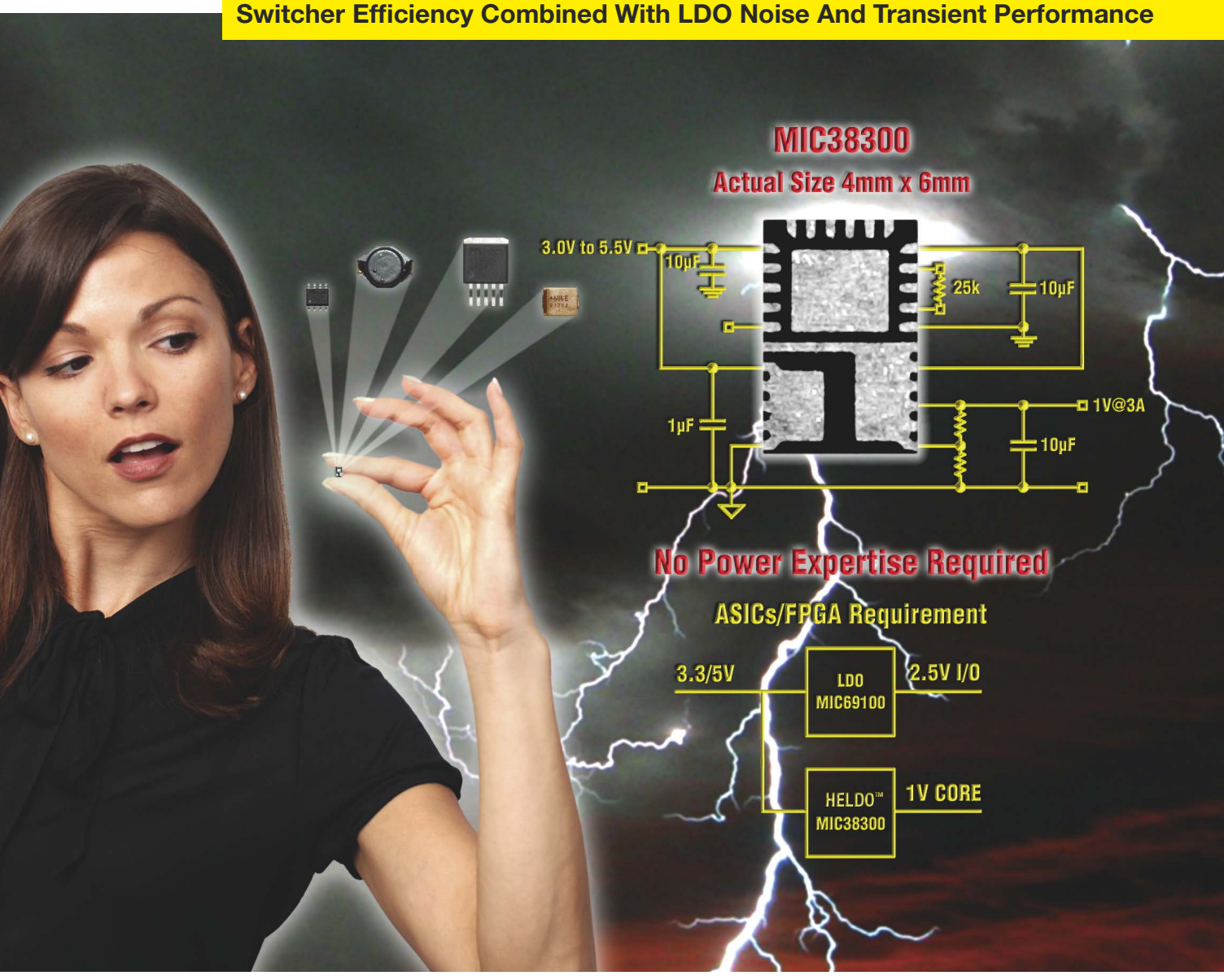

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BY LEE HILL

All about surface-mount ferrites

Simple, two-terminal SMT (surface-mount-technology)-ferrite-bead components perform crucial functions in many systems. For example, one might suppress electromagnetic emissions from a power wire. Another might provide isolation between a digital circuit and a wireless transceiver. You may be surprised to learn that the performance of a ferrite bead in any power-filtering application can vary by more than a factor of 10, depending on the magnitude of dc current passing through the part during actual operation. Understanding that behavior under the influence of dc bias can help you create quieter designs and avoid drawing wrong conclusions when troubleshooting.

Manufacturers rate all ferrite beads according to a chart that shows impedance magnitude versus frequency (**Figure 1**). You normally use a ferrite bead in a series-connected noise-blocking configuration. For that application, you should select a ferrite bead with suitably low impedance at dc but high impedance at the frequencies you wish to suppress.

An example involves the 5V-dc supply voltage in a desktop electronic appliance. Assume that the 5V supply provides host power to an external USB port. You may worry that noise from inside the system due to an internal 100-MHz clock might find some low-impedance path backward through the 5V supply circuits, ultimately making its way onto an external power cable. If that situation happens, your system might fail radiated-emissions testing due to radiation from that cable. To attenuate the passage of that noise power, you place a ferrite bead in series with the output of the 5V supply.

What happens to the impedance of that ferrite bead, and hence its noise-suppressing ability, when you plug in an external, host-powered USB device? Suppose that, in a quiescent state, the filtered 5V power net draws only 100 mA. Connecting an external USB device causes the device to draw an additional 200 mA through the ferrite bead.

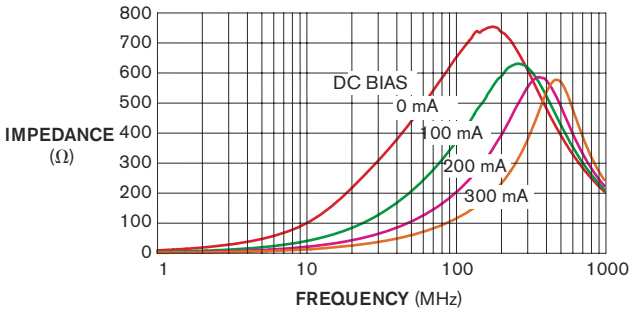

Figure 1 DC-bias current changes the performance of the ferrite bead.

Figure 1 plots a family of four curves for the ferrite bead. Each curve depicts the relation of impedance to frequency for some value of dc-bias current. An impedance bridge adds a dc bias to the device under test, generating these curves. According to the plots, changing the current from 100 mA before you plugged in the USB device to 300 mA after you plugged in the device decreases the impedance of the ferrite bead at 100 MHz from 400 to 120Ω. Assuming that the emitted radiation varies inversely with the impedance of the ferrite bead, you just increased the radiated emissions by more than 10 dB!

A casual observer might mistakenly conclude that the external USB device caused the increase in emissions. It did, indirectly, but only because the additional dc current draw modified the performance of the ferrite bead. An experienced EMI (electromagnetic-interference) troubleshooter would notice the contravening evidence that the external USB device doesn't even have a 100-MHz oscillator and the noise at 100 MHz was present before he attached the USB device.

In short, remember:

- Don't use a ferrite bead unless you have data showing impedance versus frequency while under the influence of dc-bias current.
- Don't operate ferrite beads close to their maximum rated current; impedance changes markedly as you approach the maximum rated current.
- In general, for any given level of bias current, a larger, 0805-sized ferrite bead exhibits better performance than a smaller, 0603-sized ferrite bead.

Ferrite beads can be tricky, but look on the bright side: You now have a cool little filter whose performance depends on bias current; change the bias and you can tune the filter for optimum noise suppression. EDN

Lee Hill, founding partner of Silent Solutions, teaches classes on electrical-noise reduction, conducts design reviews, and troubleshoots EMI problems. You can reach him at LHill@silent-solutions.com.

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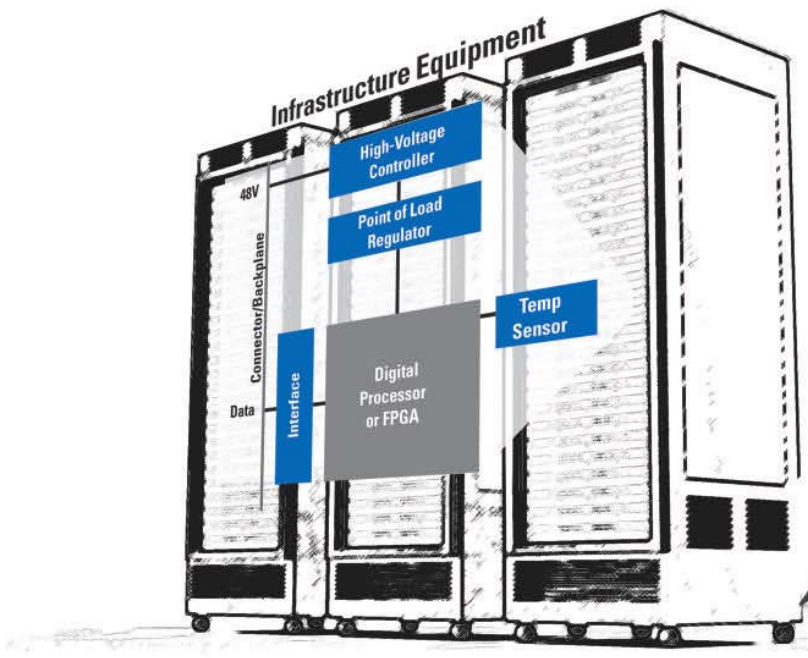

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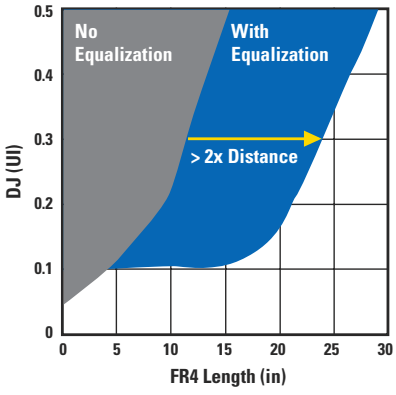

DS80EP100 12.5 Gbps Power-Saver Equalizer performance graph

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National Semiconductor

BY PALLAB CHATTERJEE, CONTRIBUTING TECHNICAL EDITOR

IP selection and power supplies

With the "greening" of electronics and IC systems, power-supply strategies are critical portions of the IP (intellectual-property)-selection process. There are two major competing power-analysis standards in the EDA world: the Accellera (www.accellera.org)-coordinated UPF (Unified Power Format) and the Cadence (www.cadence.com)/Si2 (www.si2.org)-coordinated CPF (Common Power Format). Application organizations, such as the Consumer Electronics Association, also drive power-measurement and -analysis standards. In response to the multiple formats, IP providers have not fully adopted any one side to avoid the risk of limiting their potential client bases. This failure to fully embrace just one of the standards, however, has caused confusion and uncertainty in IP users about power-strategy compatibility.

This uncertainty is a problem for several reasons. First, design groups need power-supply standards because they are trying to enhance the RTL (register-transfer-level) netlists by including power supplies in their connectivity. As a result, the design groups need to understand the source and management of the power.

More important, as the designs are going green, multimode power is key. Once again, there is variety: IP developers use several power-management techniques in different applications and for different circuits. For dynamic-power management, designers might employ simple logic optimization, clock gating, multithreshold voltage, or DVFS (dynamic-voltage and frequency scaling). Power gating, multithreshold design, and multithreshold CMOS are methods designers might employ for leakage-power management. It is difficult and consumes a great deal of conversion logic to have a large function comprising multiple IP blocks using multiple power-management techniques.

A recently emerged option for mobile and small-form-factor applications is the use of through-silicon vias.

Because there are multiple power solutions, and because these approaches have backing from different EDA vendors, you have to make sure that your IP is compatible with the EDA tools you are using. Both the UPF- and the CPF-specification formats have recommended methods, tools, and techniques for dealing with logic, clocks, and memories, as well as with other hard-IP blocks. However, the formats do not contain the same information and do not guarantee conformance or interoperability of blocks from different IP suppliers at different stages of the design process on different tools. You can obtain information from www.accellera.org/activities/upf and www.si2.org/?page=811.

From a functional point of view, the most important aspect of the power management for a design is the long-standing issue of process-isolation techniques for the applications of power. Power-reduction requirements notwithstanding, it is still important that fast-switching, high-noise power is not near or connected to high-sensitivity circuits. For that reason, designs still need multiple functional power rails for core power, memory power, I/O power, analog power, display power, and the like.

One of the last issues for IP selection—and one that designers often miss—is the type of package that will house the end product. Traditional designs employ edge-oriented I/Os, which use standard interconnect techniques to get from the circuit to the power pads. A large number of high-pin-count designs use core I/O, which is a generic term for pads that are in the middle of the chip directly over active circuitry. Designs that use core I/O can have just power supplies, just signals, or both power supplies and signals on these pads. The IP blocks must accommodate the effects of the mechanical stress that both the pads and the pads' electrical-performance issues cause. A recently emerged option that is increasingly popular for mobile and small-form-factor applications is the use of TSVs (through-silicon vias) in and around IP blocks. TSVs for stacked and 3-D die interconnect have significant die-to-die modeling and verification issues. You must develop third-party IP for applications that will employ TSVs in close cooperation with the IP provider and system-design group. EDN

Contact me at pallabc@siliconmap.net.

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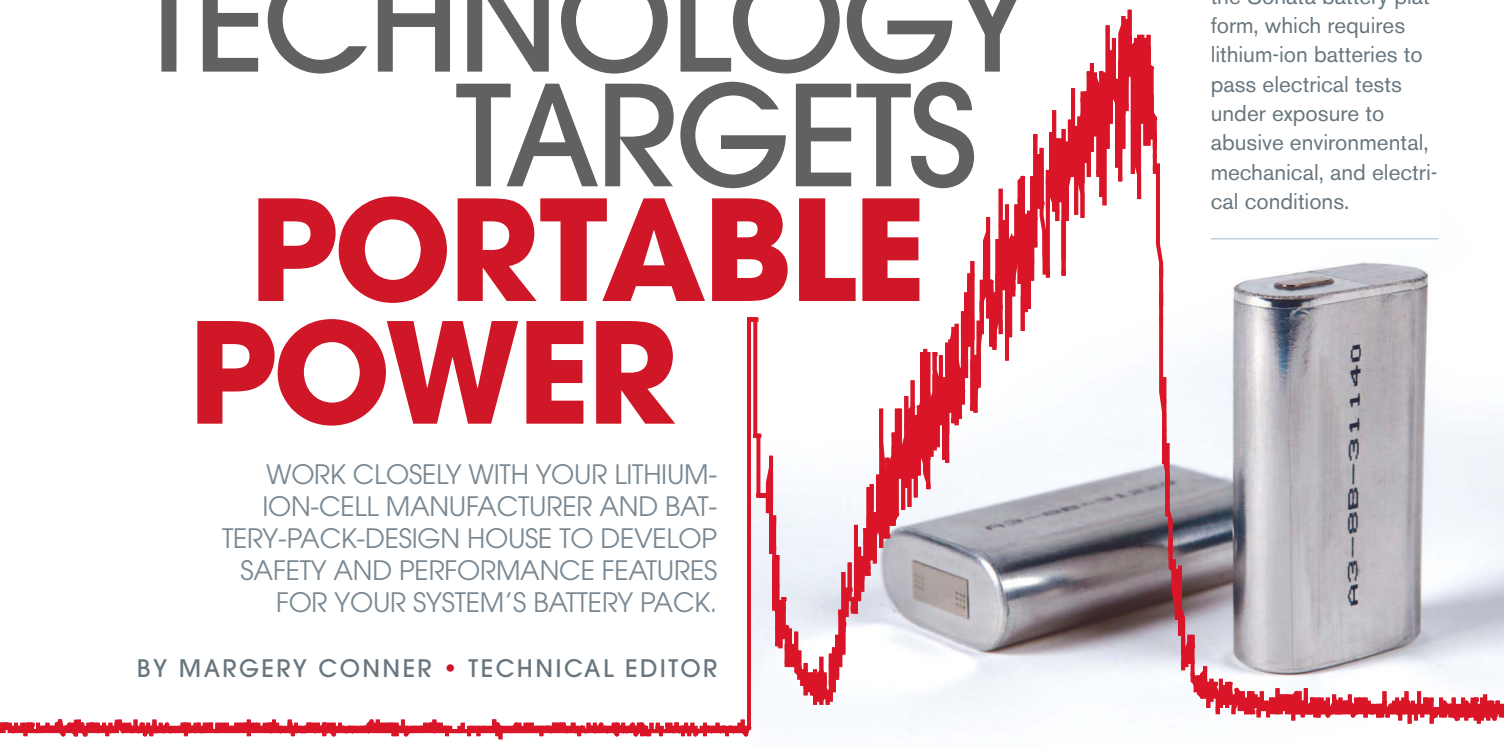
WORK CLOSELY WITH YOUR LITHIUM-ION-CELL MANUFACTURER AND BATTERY-PACK-DESIGN HOUSE TO DEVELOP SAFETY AND PERFORMANCE FEATURES FOR YOUR SYSTEM'S BATTERY PACK.

BY MARGERY CONNER • TECHNICAL EDITOR



The UL Component Program recognizes the Sonata battery platform, which requires lithium-ion batteries to pass electrical tests under exposure to abusive environmental, mechanical, and electrical conditions.

SPECIFYING, TESTING, AND MONITORING A BATTERY PACK

A typical laptop-computer battery pack can contain more than 50 Whr of energy and requires care in its design, construction, and operation to ensure that it remains safely within its operating limits. Few circuit-design engineers want or need to become battery experts, yet they must ensure that a system's battery pack can safely perform its tasks and that the host system can monitor the pack during operation. To address these constraints, you must understand how to specify a battery pack, what type of test and inspection it requires, and how the application monitors the battery pack's health during operation.

High energy capacity has made lithium ion the dominant battery chemistry for portable consumer devices (**Reference 1**). However, safety concerns also force the need for manufacturers to package the cells in a battery pack that often includes fuses, monitoring circuitry, a fuel gauge, an SMBus (system-management-bus) interface, and authentication circuitry. The industry-standard 18650 cell is about the same size as a AA battery, but even single-cell devices require that cell to be in a battery pack, complete with safety circuits and fusing.

Chemistry and technology features aside, you must select a lithium-ion-cell vendor with a stable supply chain to ensure a reliable source of packs and cells. For a variety of reasons, including recent years' massive recalls, factory shutdowns, and materials shortages, it's increasingly difficult to obtain lithium-ion cells. Couple those problems with increasing transportation costs; a poor exchange rate; increased demand for lithium-ion batteries in consumer electronics, power tools, and cars; and the rising price of cells, and you'll see why you must make a reliable supply chain a priority in selecting a cell supplier.

In the early 1990s, Sony became the first to manufacture lithium-ion cells, and the company, along with Panasonic, remains one of the largest cell vendors. Cost-sensitive, low- to medium-volume products can get by with off-the-shelf battery packs, which are available from thousands of small and midsized Chinese vendors. Don't be a penny-pincher when selecting a battery pack, however: It's seldom cost-effective to attempt to test-in quality at incoming inspection, and battery-pack field failures are dangerous liabilities. For cost-conscious, low-volume applications, an off-the-shelf pack is a valid route, but don't rely on price as the determining factor. High-volume applications can often justify

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the costs of developing a custom battery pack. In addition, low- to midsized-volume applications requiring high quality and high power, such as medical applications, can command a higher price and also can warrant a custom pack.

You can work with the battery-cell vendor or a battery-pack-design house to develop a custom battery pack. A valuable communication tool when working with your battery-pack vendor is a set of power curves that shows your application's profile over time during different operating modes, including temperature extremes. A power tool might have a discharge curve with high current spikes corresponding to cutting or drilling tasks (**Figure 1**). The magnitude and the duration of the spike vary with the shape of the material. A device that includes a radio transceiver also has spikes during transmission, and a continuous current must power its display and other functions. Ask your battery-pack vendor to demonstrate with prototype packs that its design can meet the demands you specify in all of your power curves.

Some medical-application customers of custom-battery-pack-design and -manufacturing vendor Micro Power Electronics require the company to test every battery and include a full charge-and-discharge cycle to ensure that the company has properly assembled each pack and provided it with sufficient capacity, according to Robin Tichy, marketing manager at Micro Power. In some cases, the company must develop a custom tester for the manufacturing line. Some customers require just a simple voltage test to ensure proper assembly; others require that the manufacturers perform the tests on only a sampling of products.

If your battery-pack design calls for a relatively inexpensive fuel-gauge IC that counts coulombs by calibrating the pack and by measuring the charge to and from the battery, then you must individually charge and discharge each battery pack after assembly. This calibration increases production cost and the overall battery-pack price. Tichy suggests that you weigh the trade-offs of a more expensive fuel gauge, such as Texas Instruments' Impedance Track family, which requires no initial charge-and-discharge cycle.

IEEE standard 1625 for rechargeable batteries for portable computing covers testing requirements for laptop-computer-battery packs (**Reference 2**). After Dell, Hewlett-Packard, Apple, and other laptop-computer manufac-

AT A GLANCE

- Higher-quality cells and more sophisticated battery-management circuitry can pay off in lower battery-pack-production costs.
- Battery characteristics that enhance life cycles and charge times can be differentiating features for your battery pack.
- Higher-priced as well as higher-volume products can justify the higher upfront costs of customized cells and battery packs.

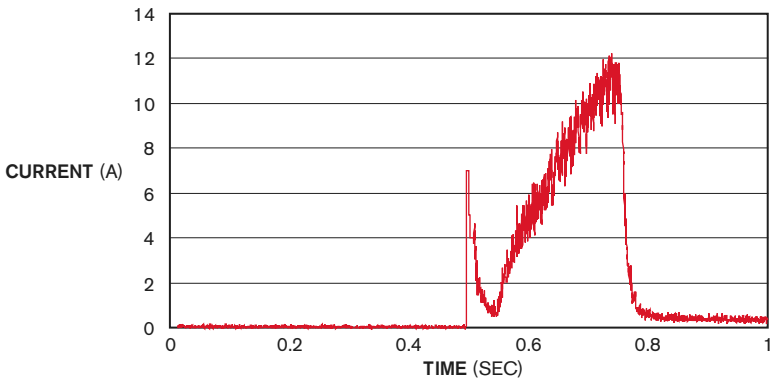

Figure 1 The system designer documents how the application uses power through power, or "discharge," curves. In this example of a battery pack for a screwdriver with a set screw, high current spikes correspond with cutting or drilling events. These events change depending on the duration of the spike and the material the drill is cutting.

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When selecting a differential amplifier, the options and features really matter. The three essential classes of differential amplifiers are the sports car, the mid-size and the economy; each class has a little something different to offer.[1]

The sports car differential amplifiers run at the highest frequencies. This class of differential amplifiers features gigahertz bandwidths, ten thousand volts-per-microsecond slew rates, a VCM pin that adjusts input and output common mode voltage, ultralow distortion, and single-ended or differential input drive capabilities. These amplifiers typically find use in broadband and IF communication applications.

The mid-size operates in the hundreds of megahertz range, has low distortion, excellent DC performance, output gain balance and phase matching, suppressing even order harmonics, high slew rate, single-ended or differential input drive capability, a VOCM pin that easily adjusts the output common mode voltage. Some models are

even available as duals. This device is used in communications and instrumentation systems to name a few applications.

The economy model comprises a pair of amplifiers integrated with gain-setting and feedback resistors in a single package, simplifying the design and saving board space. This model provides high input impedance, low power and low noise. The device is typically used with a single-ended input and has unbalanced differential outputs. It operates in the tens of megahertz range, and is usually found in low-power precision applications.

So, next time you're in the market for a differential amplifier, take a walk around the lot, kick the tires and take one out for a test ride (simulation). You'll be glad you did. As always, don't forget to read the owners manual (datasheet) front to back; it can save you a lot of time and help ensure you get the most out of your differential amplifier.

[1] To match up ADI part numbers and the various car models check out the link below.

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Contributing Writer John Ardizzoni is an Application Engineer at Analog Devices in the High Speed Amplifier Group. John joined Analog Devices in 2002, he received his BSEE from Merrimack College in 1988 and has over 28 years experience in the electronics industry.

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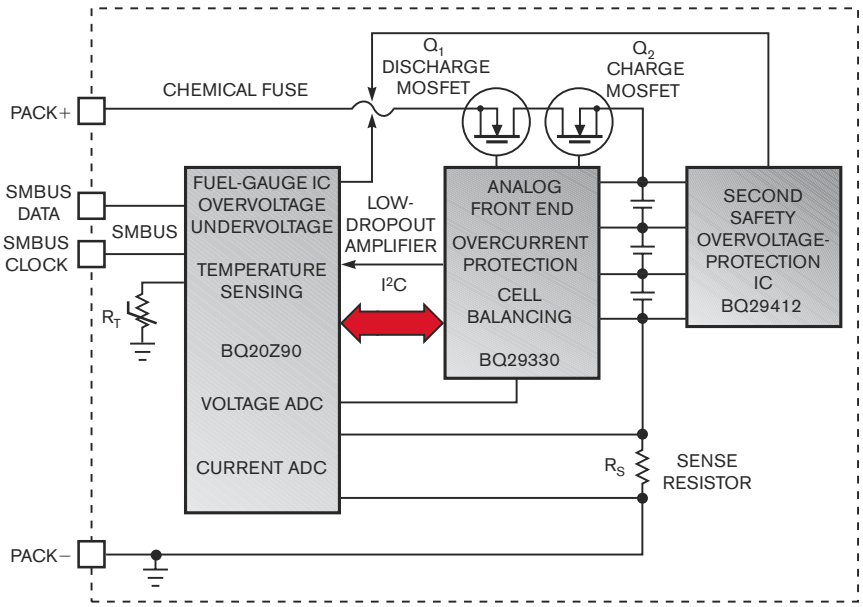

Figure 2 Smart-battery-pack electronics include a fuel gauge, an analog front end, and an overvoltage-protection IC. If the pack exceeds any of several safety conditions, such as overvoltage, overcurrent, or overtemperature, the pack can temporarily disconnect the lithium-ion cells through the safety MOSFETs or permanently disable the battery pack by blowing the chemical fuse.

turers recalled battery packs, the IEEE announced in late 2006 that it was revising the test requirements that IEEE 1625 specifies. The organization is still revising the standard and plans to release it in 2009 (**Reference 3**). Another standard, IEEE 1725, targets cell-phone and battery-pack testing. In addition, UL (Underwriter Laboratories) 1642 covers electrical, mechanical, and environmental tests for lithium-ion batteries. Rick Chamberlain, vice president of engineering at battery vendor Boston-Power, says that the industry views the UL 1642 specification as the minimum test, especially in the laptop-computer market, and most manufacturers in that segment do more testing to ensure battery-pack safety.

Battery-pack characteristics can also serve as differentiating features that your customers may be willing to pay more for or that may simply influence their purchasing decision. For example, customers may be willing to pay more for a product with a battery pack that offers a longer runtime between charges or a shorter charge time. Similarly, the total cost of ownership of a battery pack for the end user encompasses more than just the cell, power-management circuit, and packaging; it also includes the number of life cycles: More cycles mean a longer battery life.

Lithium-ion cells are not commodity items, but you can fine-tune them by varying their anode and cathode chemistry, their thickness, and their internal-separator composition. Chamberlain suggests that system designers interview cell suppliers and battery-pack designers to select the cell or even to custom-design a cell to target the performance needs and form factor of their designs. Boston-Power's initial product offering, which it announced in 2007, was the Sonata battery pack, which designers could use in available notebook-computer designs. Sonata's debut coincided with Dell's and Sony's battery recalls. Sonata's safety features included more-stable chemical reactions within the cells, proprietary current-control circuits, new thermal fuses, and pressure-relief vents.

Chamberlain points to the cell configuration within the Sonata as an example of how safety concerns complement performance needs in battery-pack design. "A typical notebook battery pack will have an arrangement of six cells in a three-series, two-parallel configura-

tion," he says. "The current splits as it goes through the paralleled cells, and, because there are slight differences in the impedance characteristics of those cells, the current goes through those cells in slightly different ways and can lead to differences in cell aging and safety concerns. The Sonata cell has a larger [than normal] format: We put three cells in series and have no parallel cells. That [arrangement] sounds relatively simple, but that type of change can offer a lot of performance and safety improvements in a battery pack."

Another example of cell customization is electrode thickness: By controlling the thickness, you can optimize for either high energy storage or high power. The leadtime for including a customized cell needn't be long: You can tweak one of the chemicals in the cell with as little as six months leadtime, according to Chamberlain. Other more significant changes could take more time. "Unless you have that discussion [with a cell supplier]," however, he says, "you'll never know."

Because a battery pack comprises electronics as well as lithium-ion cells, it's important that the system designer and battery-pack designer collaborate and understand the role the pack's power-management electronics play in ensuring both safety and performance. Smart battery packs, which can communicate with the host to report the battery's state of charge and battery-health conditions, such as life cycle, temperature, charge and discharge current, and voltage thresholds, offer the highest level of safety and performance. This electronic circuitry is usually part of the battery-pack fuel gauge, the same circuit responsible for the battery-life symbol on a laptop computer's or a cell phone's display.

A battery-pack electronic circuit can have a fuel-gauge IC; an analog front end, including overcharge protection and cell balancing; and an overvoltage-protection IC (**Figure 2**). If a battery pack's temperature exceeds a preset limit, usually 50°C, then the fuel-gauge-safety circuit will temporarily shut down the pack through one of the two charge-and-discharge safety MOSFETs that are in series with the pack cells. Once the temperature drops to within the operating-temperature range, the circuit turns the MOSFET back on, and the battery pack recovers.

You may have experienced this situation when your cell phone or laptop computer shuts down after exposure to the sun or after sitting too long in a hot car. The unit then comes back to life after a cool-down period. However, if its temperature remains high or the current remains in an unsafe range, then the circuitry can permanently disable the battery pack by blowing a chemical fuse. Once the chemical fuse blows, the pack is unsalvageable, and its next stop is the recycling center. EDN

For more on accurate lithium-ion-battery fuel gauges, go to www.edn.com/blog/1470000147/post/550029855.html.

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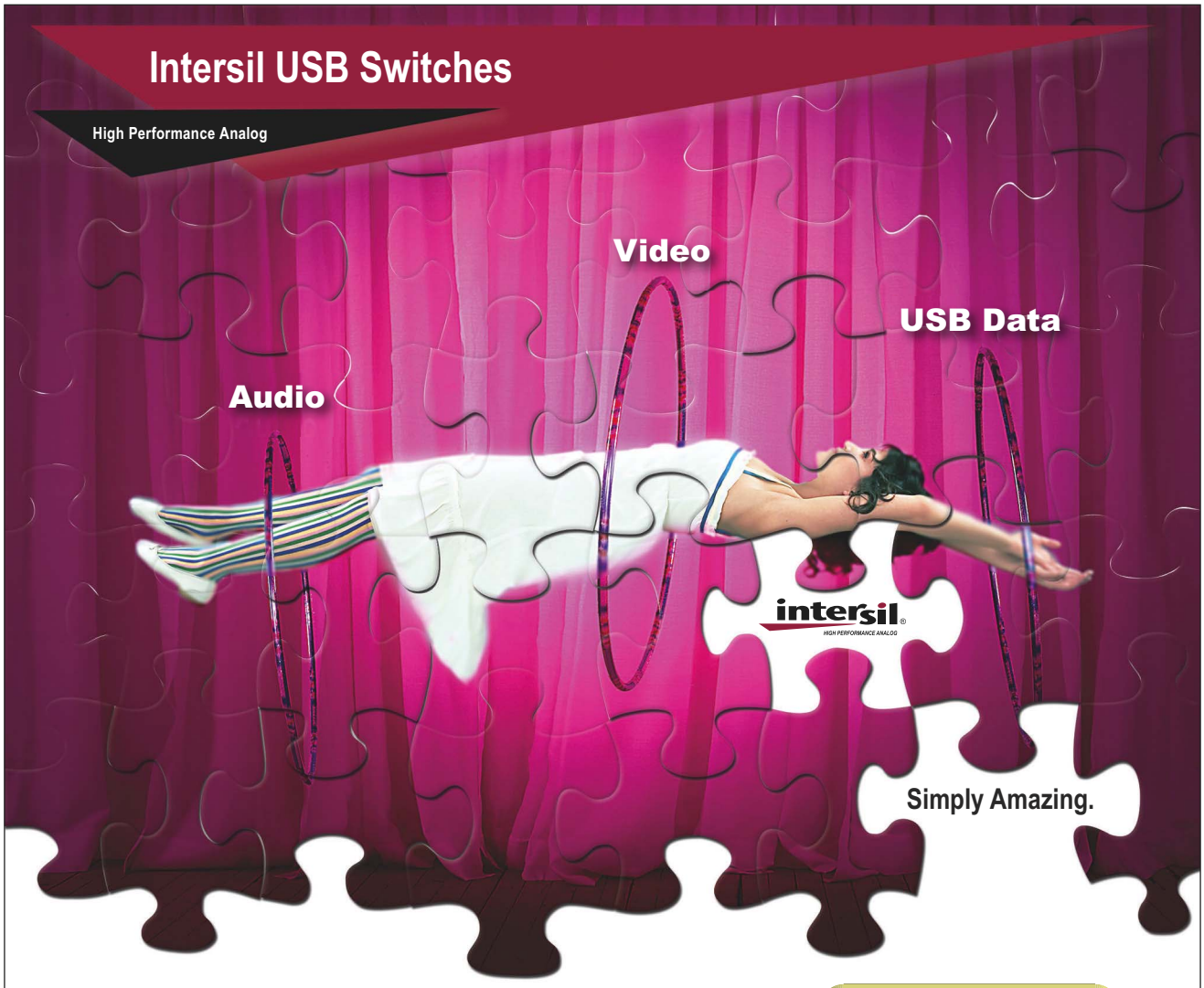

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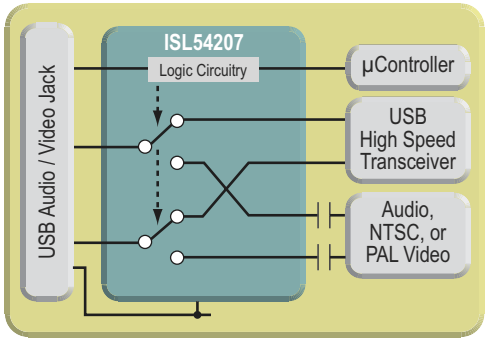

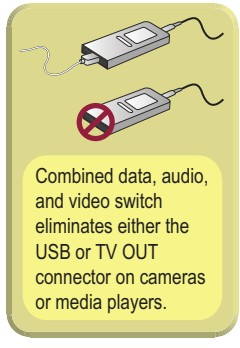

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ISL54208	0.06	480	0.28 / 0.04
ISL54415	0.007	12	0.04 / 0.03
ISL54416	0.007	12	0.04 / 0.03
ISL54417	0.007	12	0.04 / 0.03

Audio / Data

Device	Audio THD 32Ω (%)	USB Speed
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ISL54206	0.06	480
ISL54400	0.007	12
ISL54401	0.007	12
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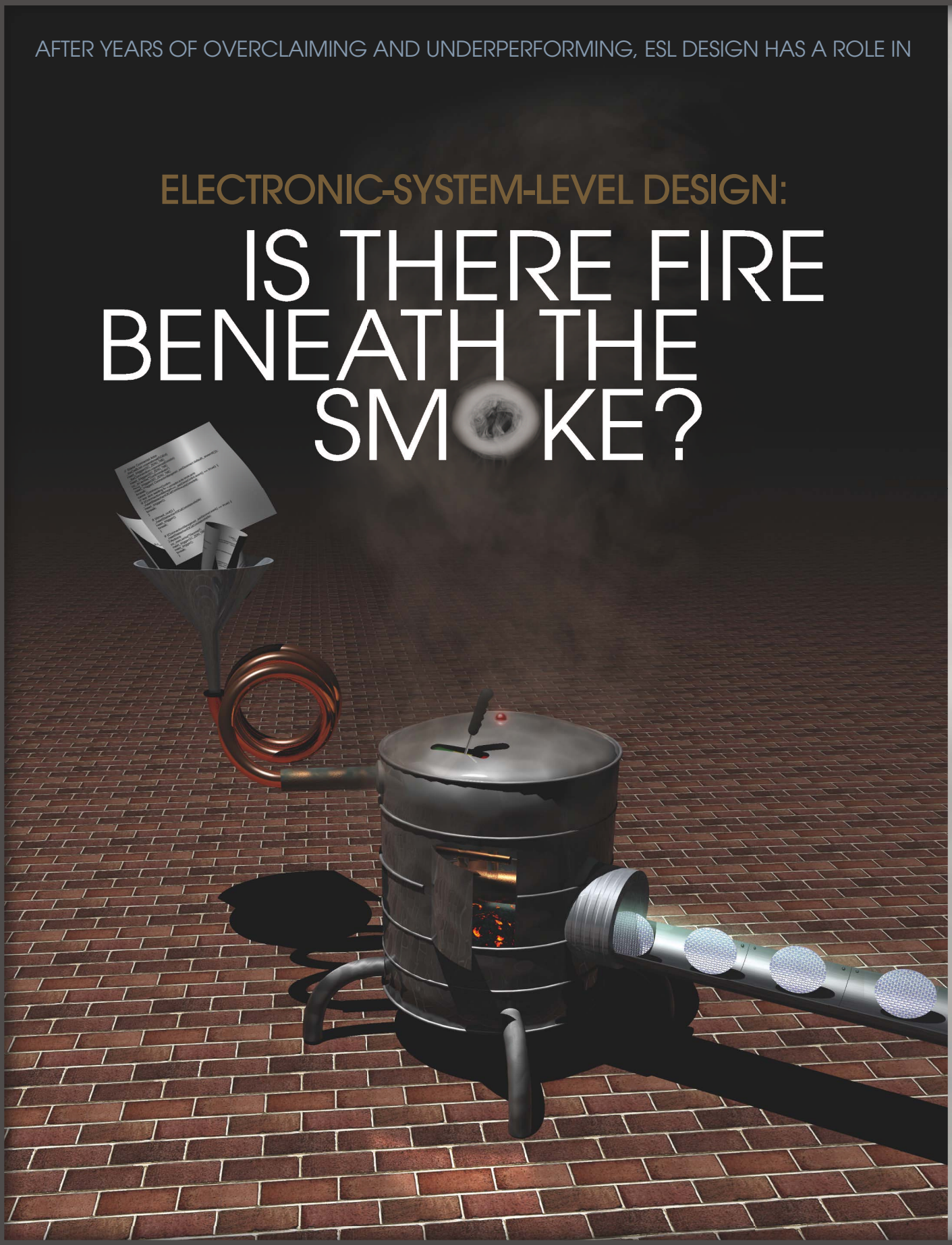

MANY DESIGN FLOWS. BUT HAS ANYONE NOTICED?

BY RON WILSON • EXECUTIVE EDITOR

It was a shimmering promise on the horizon: As SOCs (systems on chips) became more complex, we would simply move from RTL (register-transfer level) to the next-higher level of abstraction—what some experts called ESL (electronic-system-level) design. We would express the behavior of the system in a high-level language, such as C++. We would model and explore the system at that level, partition it into hardware and software components, and then push a button. Scripts and ESL-synthesis tools would digest our ESL design and give us back a nearly optimal RTL design or even a netlist together with the necessary software. Design productivity would once again be ahead of complexity.

But that was, as they say, then. Today, many failures, false claims, and too-limited tools later, many designers put ESL in the same category as gallium arsenide: a permanent technology of the future. Yet, this dismissal is as inaccurate as some of those early claims of mission accomplished. ESL tools today play key roles in many teams' design flows. Those roles differ in different teams and application areas. But the results are sufficiently important that a design manager today dismisses ESL at his own peril.

CONFUSION AND VARIETY

"In reality, most of what we call power users have been using ESL tools since about 2004," says Gary Smith, noted industry analyst and founder of Gary Smith EDA. "But many of those tools have been internally created, and there has been a lot of confusion about just what is an ESL tool."

The confusion is understandable. There are several levels of abstraction hiding under the title "system-level." And there are many kinds of tools, with different expectations, at each of those levels.

"The initial idea was that ESL was about architectural design," Smith says. This process is far simpler than pushbutton behavioral synthesis. It simply means a textual, executable representation of a system architecture that would allow experimentation at a very high level—sort of a language-based version of the time-honored architectural-design tools, the white board and the spreadsheet.

"But, in 2004, the tools were consumer-application-focused and really were for algorithm design, not architectural design," Smith continues. "There wasn't any focus on the level of abstraction that included blocks like processors and memories."

Even within the algorithm area, there were—and remain—strong differences. Some designers see an algebra-based tool such as the MathWorks' Matlab as the natural way to describe and manipulate algorithms. Others believe C or C++ should play that role, even though these languages carry a strong syntactic bias toward a particular legacy implementation—the Digital Equipment PDP-11 minicomputer. Still others believe that algorithm development should occur in a purpose-built language for describing algorithms—neither purely algebraic nor purely procedural and sequential. This last point of view nearly died out when a generation of interesting languages languished in disuse a few years ago, but it is now making a revival. "The appearance of multicore processing in the SOC world has spurred lots of new work on ESL tools," Smith observes.

A different view of ESL comes from project leaders who are simply trying to get an earlier start on software develop-

ment. In these projects, designers use ESL tools to create a software-based virtual prototype. Designers merge the prototype with, for example, driver code they are developing and test the integrated software system much as they will later test the code running on the real hardware.

Others still feel that the proper emphasis of ESL should be on the architectural level of implementation, not on simply expressing the algorithm. This notion has led to languages—primarily C-derived—and tools that attempt to describe an implementation at an abstract level and either attach to it or infer from it as much information as possible about the structure, timing, and—increasingly—energy consumption of the RTL design it implies. There has been recent work here, as well.

With all of these approaches, expectations, and needs, there is certain to be confusion. Perhaps the best way to clarify the situation is to talk with some design teams who are actually using the tools at these various levels (see **sidebar** "Look into the future").

AT A GLANCE

- Pushbutton synthesis of ESL (electronic-system-level) design to a full-chip netlist remains a dream.
- Engineers are using ESL tools in limited ways in some applications.
- System exploration and modeling can work well.
- Synthesis of algorithmic C to RTL (register-transfer level) works for datapaths.
- Tool developers are gradually expanding the ability to synthesize more-general RTL from C.

ALGORITHM DEVELOPMENT

Especially in the world of digital-signal processing, just getting the algorithm correct can be a major part of the design process. This challenge has at least two phases: getting the mathematics right and getting the translation from mathematics to hardware and software right. As Smith observes, this problem allowed perhaps the earliest successful uses of ESL tools, and it continues to be important.

Bob Davenport, DSP and system-design consultant with MC2 Technology Group, uses ESL tools in this way. He is a fan of Agilent's SystemVue, a block-diagram-driven exploration environment that finds use in signal processing in communications and media-processing applications. Davenport says that he uses the tool for developing algorithms—often assembling them from functional libraries that are part of the environment—exploring them, and then generating C code, which he then passes to Texas Instruments Code Composer Studio for optimization.

"For example, we may start with equations for a phase-locked loop, model it, and analyze its performance," Davenport says. "Then, we can generate data, graph it, and use the graphs in reports."

An important part of the capability for Davenport is that he can explore an algorithm in floating-point arithmetic with no regard to the number of significant digits and then insert tokens to set integer precision for specific signals. "So, if you are working on something like a frequency-domain GPS [global-positioning-system] correlator, for instance, you can get the core algorithm working first and then explore how to reduce the data width for implementation," he says. He can achieve this goal simply by creating a fixed-point implementation, feeding it and the original floating-point model the same inputs, and comparing the outputs. If there are differences, he probes back through the algorithm to see where they are appearing.

Davenport uses his flow primarily for generating code for DSP cores. But the package can also output hardware descriptions for FPGAs, a capability that Davenport says is less well-developed but that he intends to explore further.

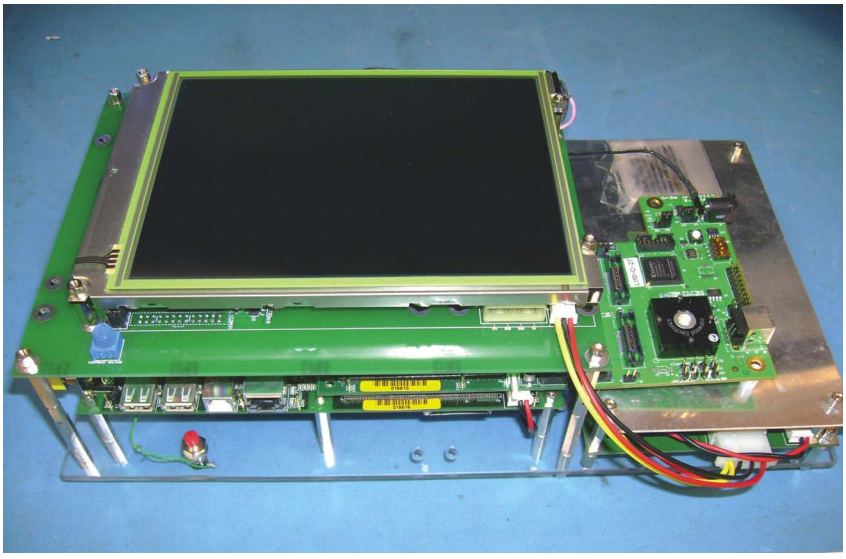

Figure 1 Synopsys designers created a SystemC transaction-level model of this development board to enable hardware/driver co-design.

VIRTUAL PLATFORMS

For some design teams, ESL is about algorithm development. For others, however, it is about concurrent hardware/software development. The IP (intellectual-property)-development group within Synopsys is a case in point. Interface IP for such interfaces as USB or PCIe (peripheral-component-interconnect express) requires driver software—not only so the licensee can use the interface, but also so the silicon team can do verification. But there is no time for the traditional approach of getting the hardware working in accordance with the specs, using the hardware to write the driver, and then using the driver and hardware to verify each other.

So, Synopsys has been using a virtual-prototyping facility from its own product line to pull driver development back in parallel with hardware development. Joachim Kunkel, vice president and general manager of the solutions group, and Joel Gotesman, R&D manager for the

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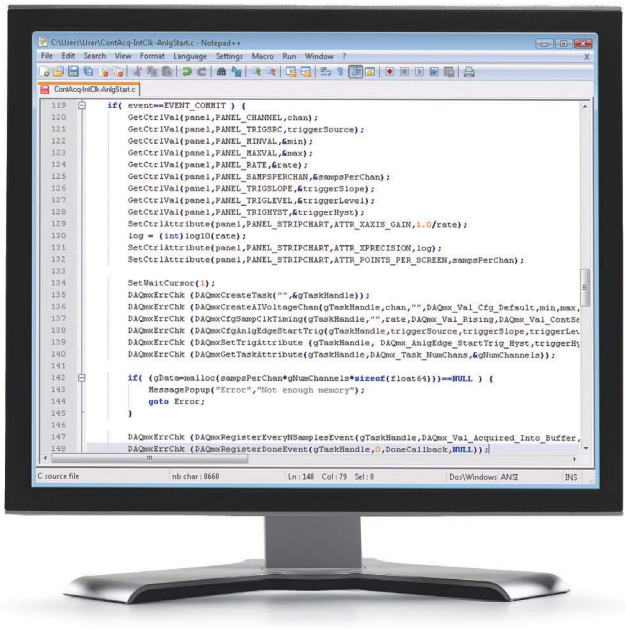

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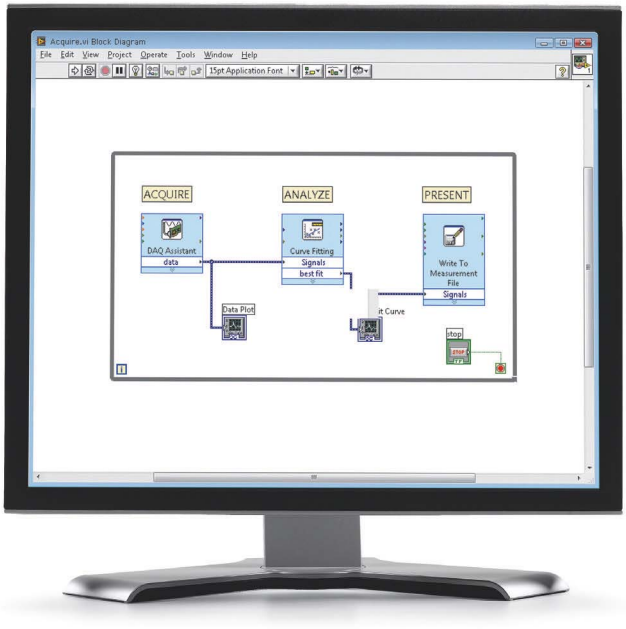

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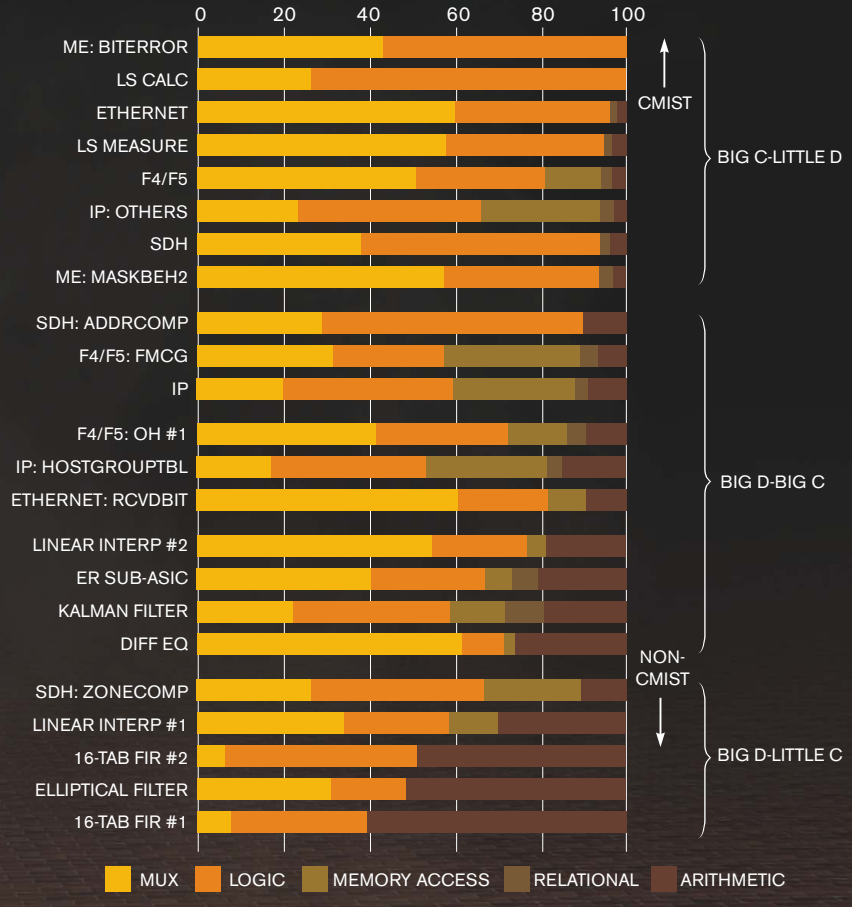
team, describe the process for a recent modification to the DesignWare USB OTG (On-The-Go) IP core.

According to Gotesman, the team started out with a hardware-evaluation board that the Synopsys DesignWare team uses widely (**Figure 1**). "The board is intended for IP-design evaluation," Gotesman explains. "It has a Samsung

LOOK INTO THE FUTURE

As the use of ESL (electronic-system-level) synthesis spreads, the next steps are coming into focus. One lingering question is how synthesis applies to nondatapath structures and to control logic. For designers whose requirements don't easily map into a traditional pipelined datapath, this issue is serious (Figure A). It appears that researchers are making progress, however.

One hopeful sign was the announcement last month of the long-rumored ESL-synthesis tool from Cadence. Cadence based the tool on work that has been going on for years at Cadence Berkeley Laboratories. The company calls the tool, somewhat inaccurately, a C-to-silicon compiler, even though it generates RTL (register-transfer-level) code. You won't know how well these claims pan out until reports start coming in from users. Companies have made such promises before. But the simple fact that Cadence is willing to boast about control-logic compilation in its introduction materials suggests that it has achieved at least an incremental improvement.



NOTE: CMIST=CONTROL- AND MEMORY-INTENSIVE SYSTEMS.

Figure A Tasks vary widely in their requirements for control, storage, and datapath functions. So, in some cases an ESL-synthesis tool's handling of control logic can be critically inportant, while in other cases it is not an issue at all.

Grant Martin, chief scientist at configurable-processor vendor Tensilica, has for years been working on the control-logic-synthesis problem. "For the current tools, the sweet spot for ESL synthesis is still datapath logic," he says. "If there is a clear exception, it might be in the networking space, where some design teams have been using [ESL-synthesis-tool set] BlueSpec in areas such as packet-classification engines."

Martin points to several issues with C-to-RTL control-logic synthesis. One is that the strategies that have so far worked best have been less dependent on C sources and not as algorithmic in their approach as the tools for datapaths. It's not that C is a poor language for expressing control logic, Martin says. Some people are comfortable using C dialects in this way. But, in C, he points out, execution time for a control algorithm is generally not an issue. In control-logic hardware, every cycle matters.

Additionally, designers who specialize in control logic have developed their own tools and flows. Switching to a new approach may not excite them unless that approach can demonstrate a substantial improvement in their productivity–without being a threat to their careers.

Still, there is the experience of networking designers who have made just this transition. Also, Martin points out, in some specialized applications, control-logic synthesis is well-established. Tensilica, which uses a proprietary synthesis tool to generate the control logic for a CPU core with extended instructions, is a case in point. "I think it's theoretically possible to do a more general tool," Martin says. "But specialized tools, such as ours, may be more common."

ARM-based chip, a display, connectors to the outside world, and an FPGA daughterboard."

The DesignWare development team some time ago re-created this board as a transaction-level model in SystemC. At this level, the model builders may represent the board as a bus with a set of functional blocks. Each block has a defined set of legal transactions it can perform with the bus and a set of functions it can perform in response to a transaction. This model becomes a software virtual-prototyping environment. Timing information is usually not in the model at this level.

In addition to the transaction-level model of the board, development teams working on new IP blocks start out by creating a transaction-level model, again in SystemC, of the IP they are developing. Combining the model of the board with the model of the IP as they would implement it in the daughterboard FPGA, the team gets a virtual prototype.

In the case at hand, the design team's job was to extend the USB OTG IP to support descriptor-based DMA (direct-memory access). Its flow allowed the team to start with the virtual prototype of the development board and the USB OTG IP and to simply modify the IP to support the new feature. This approach yielded a software virtual prototype the team could hand to the driver developers, so driver development could start almost as soon as the team nailed down the functions.

The result, according to Kunkel, is that the software team had the enhanced device driver debugged and ready to go four weeks before the hardware team had the RTL ready to program into an FPGA. At that point, Gotesman explains, the team could do a mixed-mode simulation including the transaction-level virtual prototype of the board, the RTL model of the new IP block, and the actual ARM code for the device driver. "This [approach] did require some adjustments to the SystemC code to include more timing information," Gotesman explains. From there, the team could move directly to the IP in the physical FPGA and then on to test silicon. So the ESL description of the development board in effect becomes a testbench for both the ESL description of and the RTL view of the new IP.

HARDWARE SYNTHESIS

Synopsys' use of virtual prototypes begs for one more step. Once you debug the virtual prototype, it would be great to push that magic button and synthesize the SystemC model into RTL or even into a netlist. To many designers, that scenario is the real—and unmet—promise of ESL design. But some teams are taking that approach, at least for certain kinds of structures.

One case in point is a recent project at Toshiba in Japan. Akiyoshi Oguro, LSI-division chief technology officer and group leader, and Takashi Okawa, assistant manager, describe a project to produce a hardware eigenvalue-decomposition engine from a C-language source. (Eigenvalues are sets of scalars associated with a linear system of equations.) Oguro's team is working on processing automotive-collision-avoidance radar signals using eigenvalue decomposition as a powerful but computationally intensive numerical algorithm for image recognition.

Oguro's team started with a description of the algorithm in Catapult C, evaluating three numerical techniques before settling on one for implementation. Okawa says that the presence of good math libraries—with features such as saturating integer arithmetic—is important in choosing a language for modeling at this level. Otherwise, much of the team's time will go into coding numerical methods rather than exploring the algorithm.

Using a Mentor Graphics synthesis flow, the team added architectural constraints to the Catapult C code and synthesized RTL from the result. "It's important to be able to separate the architectural constraints from the algorithm," says Okawa. "Otherwise, the two get mixed up, and you have to change your algorithmic source code to make adjustments to the implementation."

The team spent a short while examining the RTL code but moved quickly to implement it in an FPGA. They fed the FPGA real images they recorded from an automotive radar to verify the operation of the algorithm.

The ability to synthesize datapaths

from C has been around for a long time now, so it might come as no surprise that the Toshiba team succeeded. What might be less obvious is that synthesis now handles more subtle issues than just the arithmetic logic and registers in the datapath itself. One of the continuing problems with ESL synthesis—as with conventional RTL design—has been initialization sequences. It's not that hard to accidentally create a valid datapath that you can start only in simulation. But according to Oguro, the flow Toshiba used includes an auto-reset function that generated a correct initialization sequence in the RTL.

Was it worthwhile to use ESL synthesis in this case? Oguro estimates that the project would have taken about six months using conventional techniques. Using ESL synthesis, the designers had the information they needed from the FPGA in one month.

FROM DATAPATHS TO SOCs

Synthesis of a functional subblock is an important step, but today's design teams need to understand entire SOCs in which the blocks have complex interactions They also must move quickly from understanding to implementing initial RTL designs. Those problems face design teams at STMicroelectronics, long a leader in applying advanced methods, as the company develops SOCs for media-rich applications.

"Our goal is to automate the entire path between algorithm and implementation," says Pascal Urard, director of systems design at STMicro. "To [achieve this goal] we have put in place tools that take us from C++ to RTL, and we then connect to a conventional Synopsys synthesis flow."

The process begins with exploring the functions of a new design in C++. At this early stage, the team tries to estimate not only the operation of the chip design but also the throughput and latency of blocks and—critically, these days—the energy consumption. The team also begins the partitioning of functions into hardware and software.

Many architects argue that, in theory, this partitioning should happen as late as possible. But Urard warns that, with currently available tools, this approach is impractical. "Even at the system level, you don't use the same algorithms if you are targeting hardware that you do if you are targeting software," he says. Thus, the choice of target must happen early.

Power estimation is another serious issue. Urard says that, surprisingly, early power estimates are almost always within 20% of the final silicon results. "And that [situation occurs] in designs where there are lots of wires running at high frequencies," he says. "Normally, the estimates are much better than that. And, more important, the estimates of power variations are accurate."

Urard sees further progress coming in design estimation at ESL, but it will not be easy. With the growing use of aggressive and dynamic power-management techniques, estimation tools will have to pull information from low-level block and cell libraries to get enough data to form an accurate picture for a multivoltage, multimode analysis.

From estimation and system-level optimization, STMicroelectronics moves on to synthesis using Mentor tools. Urard

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admits that ESL synthesis today works better for datapaths than for control structures. But he does not see that issue as huge. "Datapaths are the main problems for us in SOCs," he says. "Much of our control logic is actually embedded in the algorithms, so it does get synthesized. And the tools we have can generate control logic for standard interfaces, as well. So, the only real issue is control structures [neither] embedded in the algorithmic portion of the logic nor defined by an interface protocol."

There are some other issues with the synthesis process, though. One involves the sensitivity of the synthesis process to coding style. "Small changes in C++ can result in huge changes in the RTL," Urard warns. "So, you have to learn to code for synthesis. You end up writing code that is more like Matlab than it is like software. On the other hand, however, you don't want to end up writing RTL in C, either. Fortunately, we have several years' experience at this [type of work]. We have found that it really takes a new engineer about one project to learn to code effectively for RTL synthesis.

"The situation is very like the early days of RTL," Urard continues. "Back then, you didn't dare put a multiplication symbol in your code. If you wanted a reasonable netlist, you wrote out the adds and shifts in RTL in just the right way. It's the same now with ESL. You have to take into account the way the synthesis tool works."

Another issue is more human than algorithmic. The next step after synthesis is verification. In STMicroelectronics' flow, that step means as much as possible formal verification of the equivalence of the C++ and RTL designs. And that verification requires that the designers, as they code the C++ for synthesis, also create constraints files for the formal verification tools.

Verification itself runs up against a couple of additional issues, Urard says. First is that perennial problem of formal tools: capacity. "We must verify very-large IP blocks," Urard observes. "We are always looking for tools with larger capacity." The other limitation is more difficult: Formal verification can prove the functional equivalence of a C++ and an RTL block. But it can't verify the scheduling or the timing. The design still has to go through conventional verification with timed models.

Is the flow delivering? Urard says that STMicro will move forward, not retreating from its use of ESL synthesis. "We are seeing four to five times the productivity using this flow, compared with designing in RTL," he reports.

Based on the experiences of these design teams, it seems clear that ESL design exploration, synthesis of datapath structures, and, to some extent—with senior and experienced people—synthesis of entire IP blocks have all established themselves in real design environments. ESL tools are no longer the pushbutton magic of marketing dreams. They are real and making an important contribution in the shops that have taken the time to learn and adjust to them. For many teams, ESL is no longer tomorrow's answer; it is today's.**EDN**

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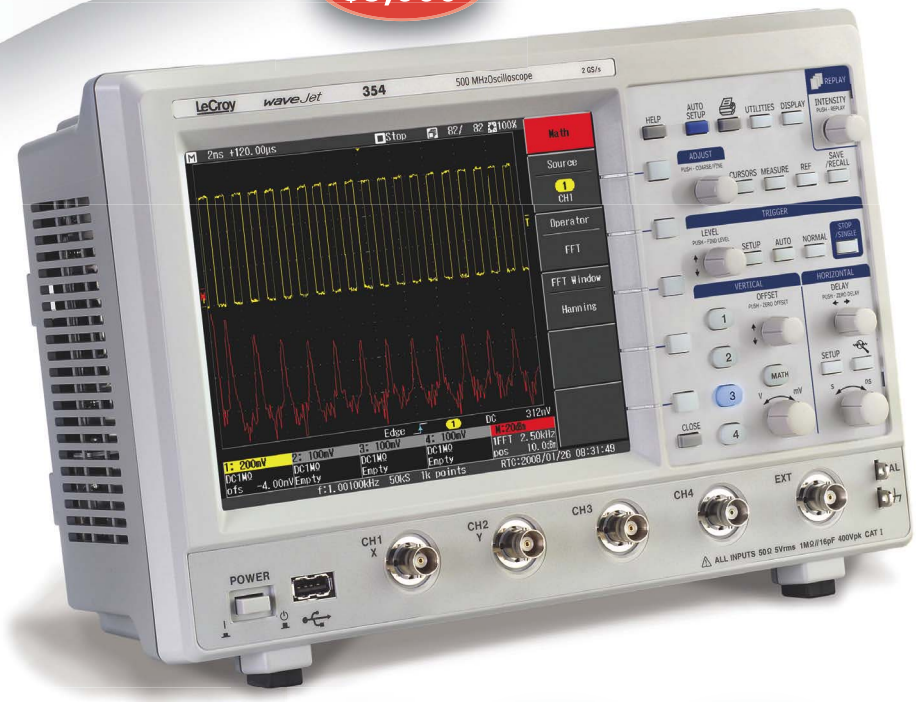

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BY NAVRAJ NANDRA • SYNOPSYS INC

On-chip test capabilities solve the analog-test problem for high-speed serial interfaces

INCLUDING ANALOG-TEST HARDWARE IN AN SOC PROVIDES VISIBILITY INTO THE PERFORMANCE OF ON-CHIP SERIAL LINKS, HELPING TO ENSURE SIGNAL INTEGRITY AND REDUCE THE COST OF MANUFACTURING TEST.

A small amount of on-chip analog-test hardware offers big payoffs when you are dealing with high-speed serial interfaces. As part of the serial-interface IP (intellectual property) or of an IP wrapper, the test hardware can provide views of the interface's performance that are more accurate than those of expensive external test equipment. As high-speed serial interfaces increase in speed, on-chip diagnostics will be the only way to verify that serial links—particularly the PHY (physical) interface—are working correctly at the designated speed.

Even today, interfaces such as PCIe (peripheral-component-interconnect express), SATA (serial advanced-technology attachment), and XAUI (10-Gbps attachment-unit interface) greatly benefit from the use of on-chip diagnostics to support rates of 2.5, 3, and 3.125G transitions/sec, respectively. Internal diagnostics enable a designer to observe the received eye diagrams and perform signal-integrity analysis of the link. Visibility into the on-chip signal is useful with PHY interfaces that have tunable equalization. If the point of visibility comes after any front-end equalizers in the receiver, a designer can directly observe the effects of receiver equalization. The effects of equalization are visible from transmitter to receiver.

Additionally, the on-chip diagnostics permit at-speed, mixed-signal tests during production test with low-cost digital testers, thereby eliminating the need for expensive analog-test equipment. With the right configuration, these diagnostics can reduce analog tests to a simple digital scan.

SOC-SERIAL-INTERFACE-TEST ISSUES

Serial links eliminate setup-and-hold requirements on data lines, require fewer I/O pins, and are higher performance than parallel links. These advantages come with trade-offs. For example, you must run careful signal-integrity analysis of the SOC (system-on-chip) package and PCB (printed-circuit-board) layout to minimize return loss and crosstalk. Additionally, debugging is more difficult because a standard logic analyzer cannot easily connect to a high-speed serial link. So, debugging signal-integrity issues requires expensive test equipment, such as a multigigahertz oscilloscope or a VNA (vector-network analyzer).

As serial rates increase to 5G, 6G, and even 10G transitions/sec for PCIe 2.0, SATA, and IEEE 802.3ap, respectively, bond wires in an SOC package represent a significant portion of the signal wavelength. PCB vias become more disruptive, and connectors cause more problems due to impedance mismatches. Crosstalk increases, and jitter becomes a big concern. In addition, insertion loss across a PCB backplane becomes steadily greater with frequency (**Figure 1**). Without receiver equalization and transmit pre-emphasis, the received eye can remain closed for many of these links, as an animated demonstration that you can find in the Web version of this article at www.edn.com/ms4285 dramatically shows.

For these reasons, the PCIe standard has gone through a significant evolution to make 5G transitions/sec workable. For example, board traces must be 85Ω rather than 100Ω to maximize trace lengths, and the standard calls for two transmitter-equalizer settings plus two autonegotiated speeds. Although the original 2.5G-transitions/sec PCIe interface required interoperability simulations only for calculating channel losses with a 13.2-dB maximum, the 5G-transitions/sec version requires the use of measured S parameters. Designers then use these parameters to calculate insertion loss, return loss, and crosstalk in time-based

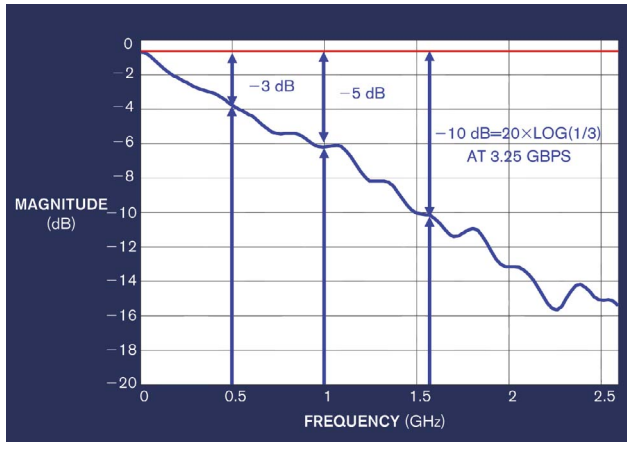

Figure 1 Off-chip factors limit the ability to measure a high-speed serial link's performance, as the insertion loss across 34 in. of FR4 PCB indicates. This loss curve was measured using a pulse-response technique that produces results similar to those you can obtain with a vector-network analyzer. The bounces indicate reflections or impedance discontinuities in the channel.

simulations. The transmitter must meet these specifications for the output and across the channel.

A simulation, even one you base on measured S parameters, is one thing. But, with the PCB-related issues of 5G- or even 2.5G-transitions/sec signals, how can a designer be sure he is receiving accurate information about a serial link's performance in an actual chip without looking at the entire channel of the silicon's transmitter-output-to-receiver input? Integrating test capabilities into the chip is the only way to avoid the distortions that may affect off-chip measurements and to see what the receiver is seeing.

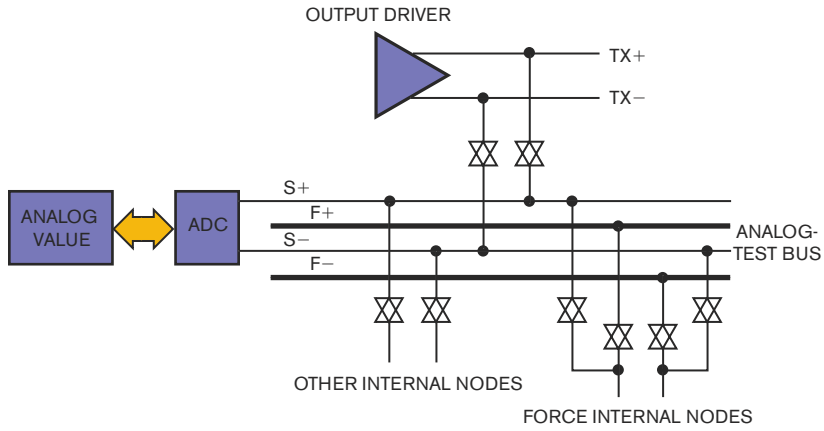

Figure 2 An on-chip analog-test bus connects to an ADC to provide the basis for complete visibility to the performance of high-speed serial links. Similar to standard scan methodologies, the analog-test bus enables scan-in of test vectors and scan-out of digitized analog values, as well as pass/fail indications from compare registers.

TEST STRATEGY

It is crucial to recognize that emerging serial links are changing the rules for dealing with high-speed data-transfer devices. Simple loop-back tests cannot reliably provide on-chip performance for links that run at speeds greater than 3G transitions/sec. Errors simply may not be measurable, in part because the SOC environment differs from that of the traditional PCB environment, which also contributes to measurement uncertainty. As University of California—Los Angeles professor Ken Yang points out, SOCs experience system-interaction-induced errors from variables such as packaging, temperature, and voltage, all of whose effects are invisible outside the chip. At sufficiently high speeds, SOCs containing serial links become untestable using traditional external testers.

A typical test suite to judge the performance of a PHY interface in a high-speed serial interface includes tests of BER (bit-error rate), asynchronous BER, transmitting voltage, eye mask, transmitter jitter, receiver offset, and received voltage level. Most of these tests rely on analog-signal measurements that an ADC can capture. Because the objective is to eliminate the possibility of signal distortions from the chip's package and other parts of the I/O channel, the chip must integrate the ADC.

Standard digital-scan methods provide a good model for creating this visibility into the on-chip performance. For digital-circuitry testing, control circuitry loads serial-scan data into registers and then scans the combinatorial results from the registers. Software tools offer comprehensive support for digital-scan methodologies, including providing help in developing test patterns and measuring test coverage. With an area overhead of less than 15% for the average chip, scan methods provide observability of internal digital signals and enable simple automated testing.

To get this same level of internal testability for analog cir-

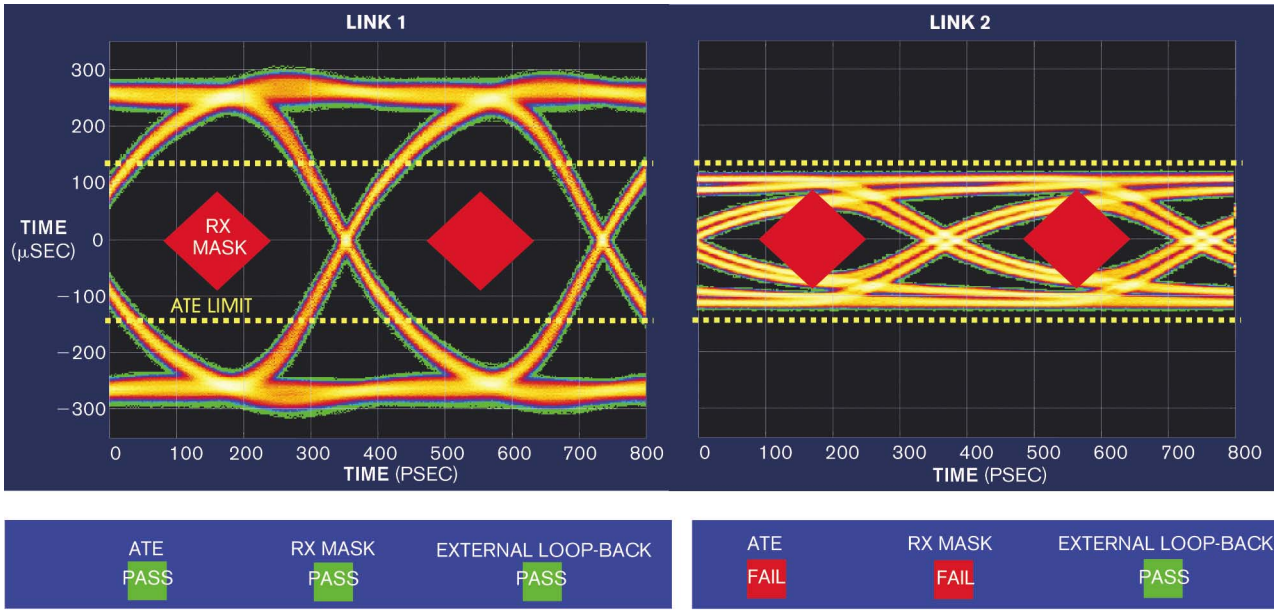

Figure 3 Traditional loop-back tests, such as this one on a PCIe eye mask, often fail to give accurate results when link speeds increase into the multiple-gigatransitions/sec range.

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cuitry, you must include some type of analog-test bus. **Figure 2** shows a straightforward analog bus that has four interconnect wires: two force lines and two sense lines. An associated four-pin JTAG interface can handle all setup and measurement tasks. Once the bus is in place, you can integrate additional resources around the analog-test bus, enabling a versatile set of built-in analog-test capabilities that can fully test the performance of a PHY interface. With resources on-chip, all external access to the PHY interface can be through a simple digital port. As the next section explains, it is possible to reduce all analog-test results to a single pass/fail bit. Using this approach, you can reduce a complete analog-test approach to the process of accessing a simple digital interface, such as JTAG, with no external analog equipment.

CONVERTING ANALOG TESTS TO DIGITAL

Measuring an analog value, such as transmitting amplitude using an on-chip ADC, results in a continuous range of acceptable and unacceptable values and, in turn, a true analog result. Once you convert this result to a digital value, a tester could read the result and convert it into a pass/fail result within a set of acceptable limits. However, this type of pass/fail testing requires someone to write a test program to read the value, convert the value, compare it with acceptable limits, and determine pass or fail requirements. Someone must also debug and maintain this test program across a variety of test platforms.

Fortunately, you can avoid this cumbersome and costly approach by handling the comparison between analog values and acceptable limits using on-chip limit registers. The first step is to simply write into the chip the high and low analog limits and the instructions to measure the desired value. Each test sets an on-chip pass/fail bit that you can then scan for a simple pass/fail comparison. You need not write a test program; you need only software to create the input and compare vectors, just as in conventional digital scan. The result of placing the limit registers and ADC on-chip is true analog testing on any simple digital tester on any test platform.

To make on-chip analog-test capabilities as easy to use as digital-scan methodologies, software tools must convert typical analog tests to digital-test patterns. The software must be able

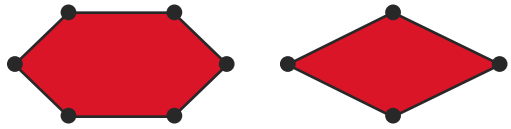

Figure 4 You can automate eye-mask tests by specifying voltage and phase values for various points on a hexagonal or diamond mask. Compare registers that connect to your SOC's on-chip analog-test bus can automatically determine whether your specified eye values match the actual values of the on-chip signals. In the six-point mask (left), the six points yield a voltage of 100 mV and a phase of 0.2 unit intervals, a voltage of 100 mV and a voltage of −0.2 unit intervals, a voltage of −100 mV and a phase of 0.2 unit intervals, a voltage of −100 mV and a phase of −0.2 unit intervals, a phase of 0.4 unit intervals, and a phase of −0.4 unit intervals. A four-point mask (right) yields a voltage of 100 mV, a voltage of −100 mV, a phase of 0.4 unit intervals, and a phase of −0.4 unit intervals.

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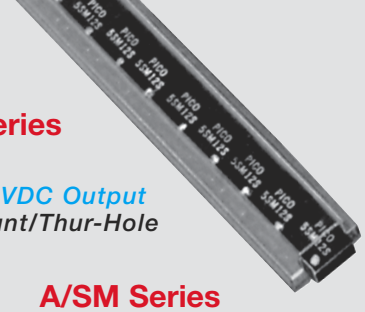

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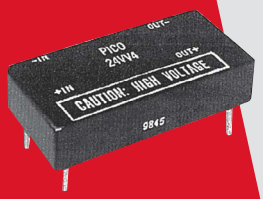

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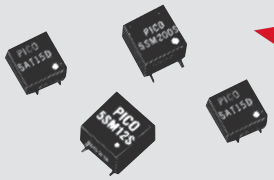

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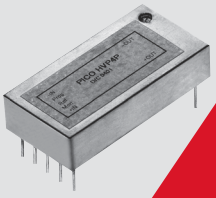

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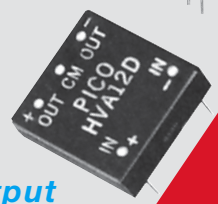

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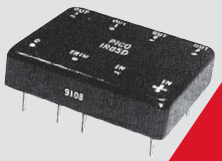

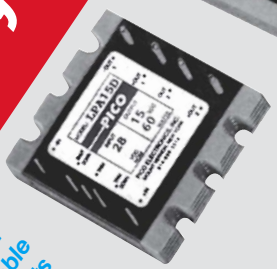

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to generate pass/fail tests that would otherwise require a large amount of configuration and circuit knowledge.

With the increasing availability of PHY interfaces as IP, the IP industry must implement digital testing of emerging serial interfaces in a straightforward way. This implementation will allow IP users to quickly assemble complete analog-test suites without an in-depth knowledge of the IP or of a serial-interface standard.

As an example of such a test implementation, consider the typical eye-mask test. The relevant interface standard specifies eye masks that provide a starting point, but designers usually use a larger mask to account for channel distortion and to ensure interoperability (**Figure 3**). Using a diamond or hexagonal mask, a designer specifies pass/fail values for voltage and phase for each point on the mask (**Figure 4**). The software then generates the appropriate vector to place the device in the proper configuration and applies the specified mask. The SOC then returns a pass/fail result. This approach to testing requires no device knowledge.

FULL-TIME VISIBILITY

In addition to providing a low-cost test method, on-chip test also allows for in-the-field debugging and testing. Circuitry should display eye diagrams at the receiver and measure various other critical parameters. This capability provides an easy method to help evaluate field issues. With transmitter pre-emphasis and receiver equalization becoming ever more popular, the ability to measure the effects of various settings on a link at any time is valuable.

The conventional approach of production testing using simple external loop-back is fast but inaccurate. On the other hand, expensive, sophisticated mixed-signal testers burden users with additional overhead costs and the need to write and debug complex test programs. With the help of on-chip analog-test circuitry, you can test high-speed serial interfaces at speed on a low-cost digital tester in little time. As a result, you can generate verified pure-digital test patterns for compliance tests and other requirements, including eye mask, asynchronous-voltage margining, and transmitter-level testing. Further, you can use this same circuitry to aid in debugging and characterizing such interfaces. EDN

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AUTHOR'S BIOGRAPHY

Navraj Nandra is currently director of product marketing for Synopsys' mixed-signal-IP-solutions group. He has worked in the semiconductor industry since the mid-1980s as an analog- and mixed-signal designer for Philips Semiconductors, austriamicrosystems, and EM-Marin and was director of application engineering at Barcelona Design. Nandra holds a master's degree in microelectronics from Brunel University (Middlesex, UK) and a postgraduate diploma in process technology from Middlesex University (Middlesex, UK). He has presented at numerous technical conferences on mixed-signal design, analog IP, and analog-synthesis EDA. Nandra also maintains a blog on mixed-signal IP at http://synopsysoc.org/theeyeshaveit.

LINEAR TECHNOLOGY

DESIGN NOTES

12-bit DAC in TSOT-23 Includes Bidirectional REF Pin for Connection to Op Amp or External High Precision Reference

Design Note 448

Kevin Wrenner, Troy Seman and Mark Thoren

Introduction

The LTC®2630's combination of a 12-bit DAC and low-drift integrated reference in a tiny SC-70 package has proven popular for a wide variety of applications. Two new DACs, the LTC2631 and LTC2640, take this winning formula and further expand its reach by adding a bidirectional REF pin and an optional I²C interface in a tiny TSOT-23.

Like their predecessor, these parts feature 1-bit INL and DNL, offer excellent load regulation driving up to 10mA loads, and can operate rail-to-rail. See Table 1 for a list of options.

Applications Using REF Pin

The bidirectional REF pin can be used as an output, where the accurate 10ppm/°C reference is available to the rest of the application circuit, or it can be used as an input for an external reference.

To configure REF as an output, simply tie the REF_SEL pin high. As an output, the REF pin simplifies pairing the DAC with an op amp. For instance, to achieve an output range centered at 0V, drive the plus input of the op amp, with REF connected to the minus input. Avoid loading the REF pin with DC current, instead buffer its 500Ω output with an LTC2054 or similar precision op amp.

The LT1991 precision op amp is a superb choice for amplifying or attenuating the DAC output to achieve a desired output range because it requires no precision external resistors. Its integrated, precision resistors are matched to 0.04%, allowing gain to be set by simple pin strapping (see the data sheet for a large variety of gain options). Figure 1 shows the configuration for a difference gain of 4, resulting in a ±5V output with 12-bit programmability under I²C control. Integral nonlinearity, seen in Figure 2, is better than 1LSB.

Figure 3 shows a negative output system using a similar setup, this time with the LT1991 configured as an inverting amplifier with a gain of –0.25. The 0.1µF capacitor at REF reduces the already low DAC noise by up to 20%.

For applications requiring more accuracy at full scale, the LTC2631 and LTC2640 can be referenced to an external source. Figure 4 shows how, using an LT1790 low-dropout reference that's accurate to 0.05%. Tying REF_SEL low configures the REF pin as a reference input. If reset-to-zero is needed, an LTC2640-LZ12 can be substituted. (For that option, pin 8 is rededicated as a $\overline{CLR}$ pin, and, upon powering up, External Reference mode must be selected by software command before the code is changed from zero.)

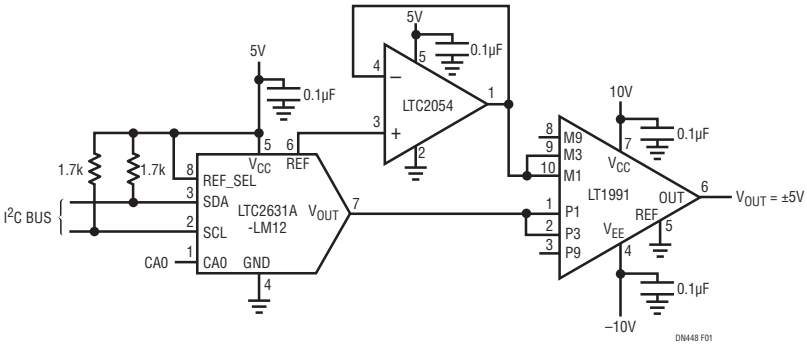

Figure 1. Programmable ±5V Output

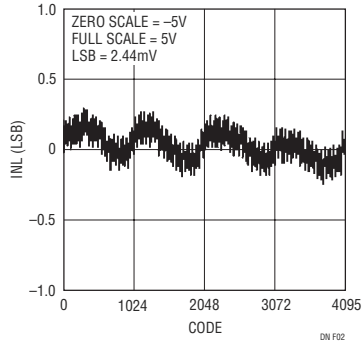

Figure 2. Integral Nonlinearity of Programmable ±5V Output

The REF pin enables the LTC2631 and LTC2640 to share their full-scale range with another device, as shown in Figure 5. A 16-bit LTC2453 ADC and LTC2631 DAC are referenced to the same 5V full scale. This circuit allows a variety of possible transfer functions to be applied to an input under computer control. It is easy to implement functions such as squaring and square root, or time-dependent functions such as integration or proportional-integral-derivative (PID) control in this manner, resulting in a circuit that is much simpler and more stable than a purely analog circuit.

Conclusion

The LTC2631 and LTC2640 add I²C capability and a bidirectional REF pin to LTC's family of 12-, 10-, and 8-bit DACs with an integrated reference. For applications requiring a modified output range, the LT1991 op amp with internal precision resistors is an ideal counterpart.

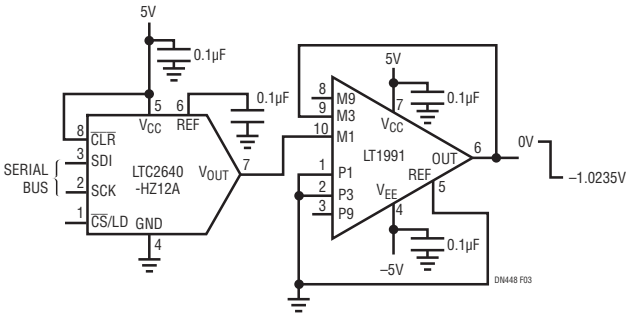

Figure 3. Negative Output, 0V to –1.024V

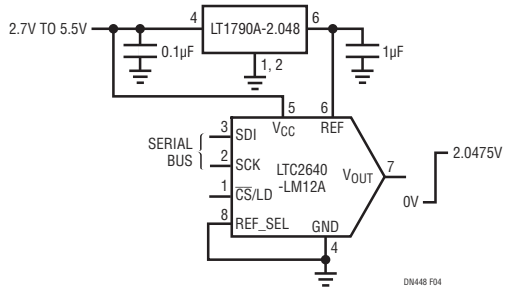

Figure 4. 0V to 2.048V Output Derived from External Reference

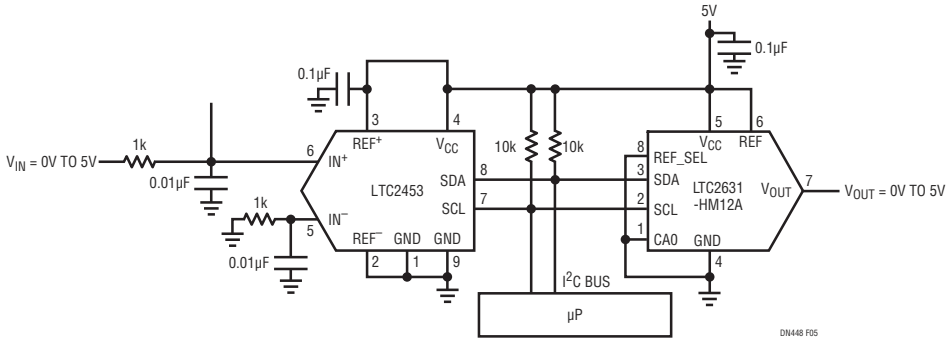

Figure 5. Electronic Transfer Function Generator

Table 1. Family Characteristics. Each part has a bidirectional REF pin and is available in 12-, 10-, and 8-bit accuracy

PART NUMBER	TYPE	FULL- SCALE	POWER-ON RESET CODE	PIN 8 FUNCTION
LTC2631-LM	I²C	2.5V	Midscale	Select default REF
LTC2631-LZ	I²C	2.5V	Zero	6 add'l addresses
LTC2631-HM	I²C	4.096V	Midscale	Select default REF
LTC2631-HZ	I²C	4.096V	Zero	6 add'l addresses
LTC2640-LM	SPI	2.5V	Midscale	Select default REF
LTC2640-LZ	SPI	2.5V	Zero	DAC Clear
LTC2640-HM	SPI	4.096V	Midscale	Select default REF
LTC2640-HZ	SPI	4.096V	Zero	DAC Clear

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Part No.	Buck (I_{OUT})	Boost (I_{SW})	Buck-Boost (I_{OUT})	LDO (I_{OUT})	Package (mm)
LTC®3544	300mA + 200mA + 200mA + 100mA				3 x 3 QFN-16
LTC3562	600mA + 600mA + 400mA + 400mA				3 x 3 QFN-20
LTC3445	600mA			50mA + 50mA	4 x 4 QFN-24
LTC3670/72	400mA			150mA + 150mA	2 x 3 DFN-12 / 2 x 2 DFN-8
LTC3100	250mA	800mA		100mA	3 x 3 QFN-16
LTC3446	1A			300mA + 300mA	3 x 4 DFN-14
LTC3541	500mA			300mA	3 x 3 DFN-10
LTC3545	800mA + 800mA + 800mA				3 x 3 QFN-16
LTC3522	200mA		400mA		3 x 3 QFN-10
LTC3520	600mA		1A	LDO Controller	4 x 4 QFN-24
LTC3537		600mA		100mA	3 x 3 QFN-16
LTC3523	400mA	600mA			3 x 3 QFN-16
LTC3527		600mA + 400mA			3 x 3 QFN-16
LTC3547	300mA + 300mA				2 x 3 DFN-8
LTC3419	600mA + 600mA				3 x 3 DFN-10, MS10
LTC3548	800mA + 400mA				3 x 3 DFN-10, MS10E
LTC3407A-2	800mA + 800mA				3 x 3 DFN-10, MS10E
LTC3417A-2	1.5A + 1A				3 x 5 DFN-16, TSSOP-20E

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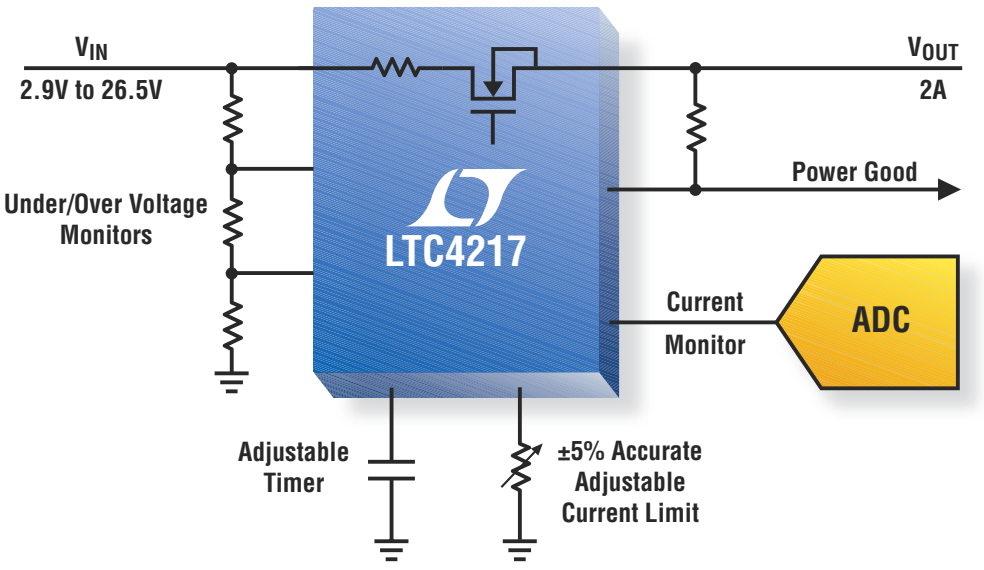

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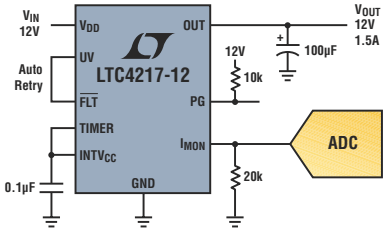
LTC4217-12 Dedicated 12V Version



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READERS SOLVE DESIGN PROBLEMS

Astable multivibrator lights LED from a single cell

Luca Bruno, ITIS Hensemberger, Monza, Lissone, Italy

Lighting LEDs from a single 1.5V cell poses a problem because their forward voltages are higher than the cell's. The simplest way to light the LED is to use a step-up dc/dc converter. This Design Idea offers a simple and reliable alternative for applications in which low cost is of primary concern. The circuit in **Figure 1** employs a classic astable oscillator, which transistors Q_1 and Q_2 form. The square-wave drive signal at Q_2's collector turns a PNP switching transistor, Q_3, on and off. When Q_3 turns on, it charges inductor L_1, and, when it turns off, inductor L_1 discharges its stored energy through the LED during flyback, allowing you to light any type or color of LED.

The astable circuit oscillates at a frequency of $1/T_O$, where $T_O=T_L+T_H$ with $T_L \simeq 0.76R_2C_2$ and $T_H \simeq 0.76R_1C_1$ when the cell voltage is 1.5V, where T_O is the time, T_L is the on-time, and T_H is the off-time. With the component values in **Figure 1**, the frequency and the duty cycle are about 28.5 kHz and 50%, respectively. During the on-time, transistor Q_3 is on, and inductor L_1 starts to charge with constant voltage so its current ramps up linearly to a peak value, as the following **equation** describes: $I_{L1PEAK}=[(V_{BAT}-V_{CESATQ3})/L_1]\times T_L$, where I_{L1PEAK} is the peak current of L_1, V_{BAT} is the battery voltage, and $V_{CESATQ3}$ is the collector-to-emitter saturation voltage of Q_3. During the off-time, Q_3 is off, and the inductor's voltage reverses polarity, forward-biasing the LED and discharging through it at a constant voltage roughly equal to the forward voltage of the LED while its current ramps down to zero.

Because this cycle repeats at a high rate, the LED appears always on. The LED's brightness depends on its own average current, which is proportional to the peak value. Because the LED current is roughly a triangular pulse with a peak current approximately equal to the inductor's current because of the finite turn-off time of Q_3, you can easily estimate the average current: $I_{LEDAVG} \simeq (½)\times I_{L1PEAK}\times(T_{DIS}/T_O)$, where T_{DIS} is the discharge time of inductor L_1 through the LED, which you can roughly estimate from the slope of L_1's discharge, which is V_{LED}/L_1, where V_{LED} is the LED's voltage.

To control the LED's brightness, you may increase or decrease the inductor's peak current by varying its inductance from 100 to 330 µH to achieve the optimal brightness for the type of LED you are using. However, L_1's charge slope is always smaller than its discharge slope, and, because T_L and T_H are equal, L_1 has enough time to discharge completely. When it recharges on its next cycle, its current

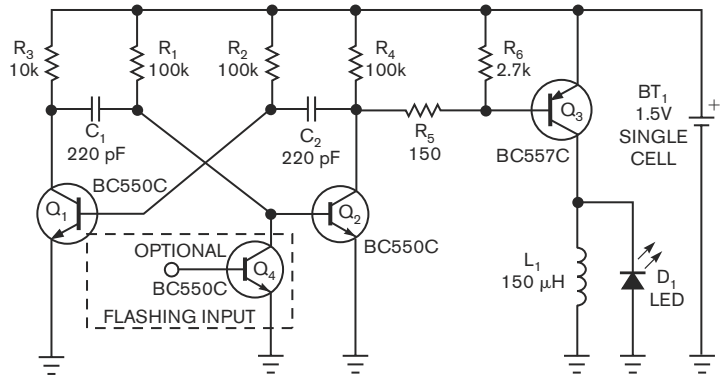

Figure 1 This simple astable multivibrator provides a low-cost way to drive an LED from a single cell.

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cycle always starts from zero. If this is not the case—if you reduce T_H too much, for example—the inductor current increases on each cycle until Q_3 goes out of saturation, and the final current value becomes unpredictable because it depends on Q_3's dc gain. Optional transistor Q_4 allows the circuit to flash the LED when a low-frequency gating signal drives its base.

No one component is critical; for example, any small-signal transistor is suitable. But, if possible, choose a PNP transistor for Q_3 with high dc-current gain and low collector-to-emitter saturation voltage for best efficiency. Also, take care that the peak current does not saturate L_1 and does not exceed the maximum peak-current rating of Q_3 and the LED. The astable circuit starts to operate with a supply voltage as low as 0.6V, but the LED is off and begins to light dimly when the supply voltage exceeds 0.9V. When the supply voltage exceeds 1V, the LED's brightness is adequate, even if it depends slightly on the forward voltage of the LED. EDN

IC provides versatile toggle functions

Louis Vlemincq,
Belgacom, Evere, Belgium

The circuit in **Figure 1** offers not only as many as six channels in a single IC package, but also a high level of additional flexibility. The configuration of Output 1 is a "plain-vanilla" toggle. A resistive divider comprising R_1 and R_2 provides a midsupply bias to all the channels through resistors R_3, R_6, R_7, R_{10}, and R_{12}. Because the bias voltage of R_1/R_2 is within the hysteresis range of the gates, they behave as flip-flops, retaining their high or low state in a stable manner.

Debouncing capacitors C_2, C_3, C_4, and C_5 charge to the level of the output. Pushing switch S_1 inverts the output state because of the inverting action of the gate. This state remains stable because, in the first gate's circuit, for example, R_4's value is larger than that of R_3, and R_4 cannot overcome the hysteresis threshold of the gate. Only the discharge of C_2 can accomplish that task. When you release the pushbutton, C_2 fully charges after the debouncing delay, and the circuit is ready for another inversion. C_1 provides a general power-on-reset feature to all the channels. If your circuit requires only one channel, you can directly connect R_1 and R_2 to the input of the gate, omitting R_3.

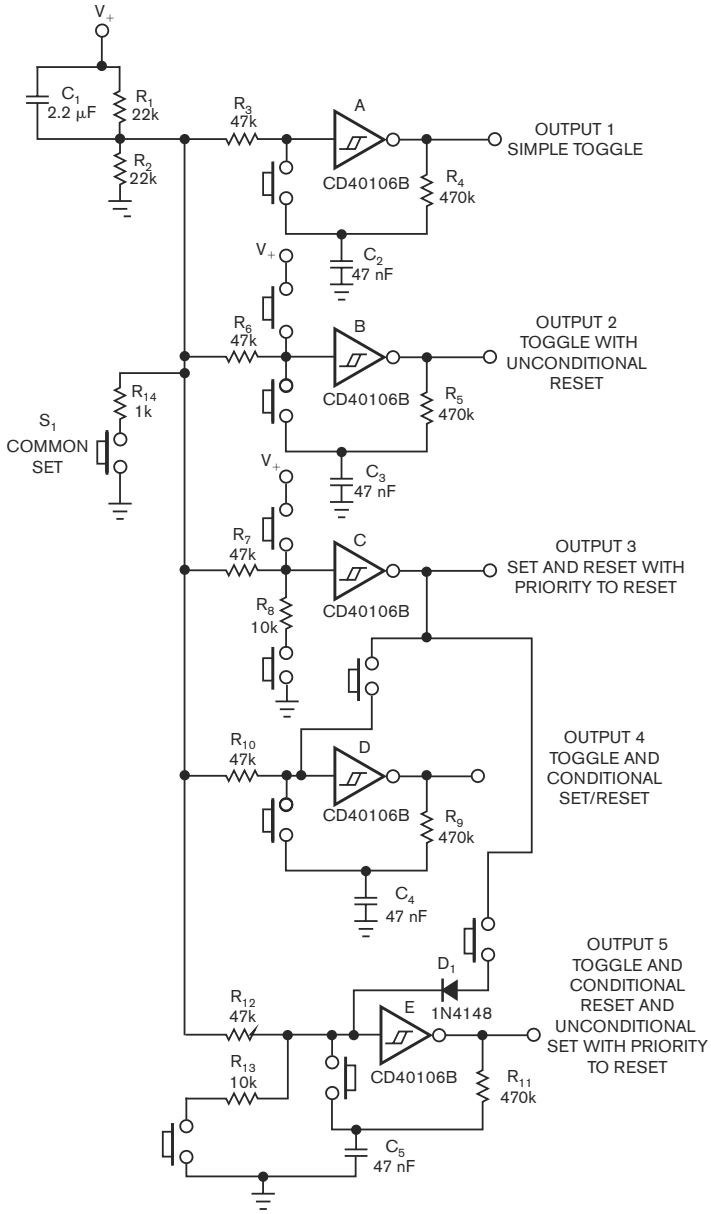

Figure 1 This circuit shows multiple Schmitt-trigger inverters functioning as a variety of set/reset toggles.

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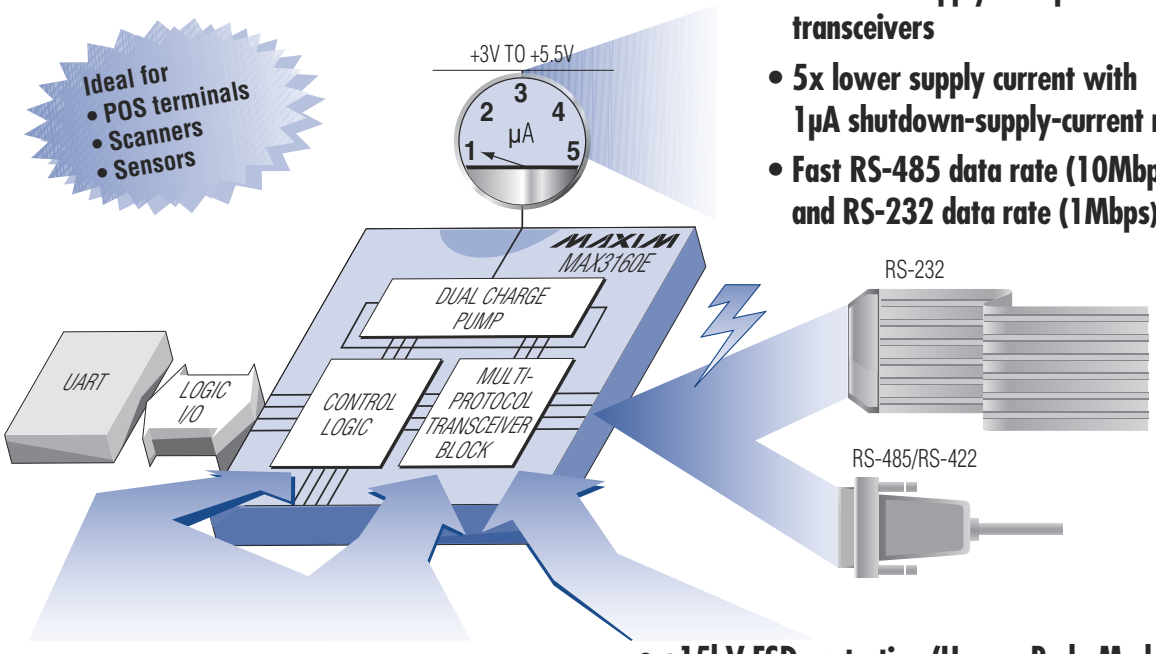

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MAX3162E	Dedicated 2Tx/2Rx RS-232 and 1Tx/1Rx RS-485/RS-422	256	28-SSOP	

†1000-up recommended resale. Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates. Not all packages are offered in 1k increments, and some may require minimum order quantities.

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Output 2 has the same toggle function as Output 1 but also includes a direct reset. Output 3 works only in a set/reset mode; the position of R_8 determines the priority state. Output 4 also has a toggle action, but you can set or reset it to a state opposite that of Output 3. Output 5 works in a similar manner, except it allows only a conditional reset because of the position of D_1. Output 5 also includes a forced, nonpriority set. You can mix and match all these functions, providing almost unlimited versatility.

The IC in **Figure 1** is a Fairchild Semiconductor (www.fairchildsemi.com) CD4000-series circuit, suitable for supplies of 3 to 15V, but it could also be a 74AC14 or 74HC14 from NXP (www.nxp.com), for example. Any CMOS-input gate having a Schmitt-trigger action is suitable. You must take care to bias the inputs in the middle of their hysteresis range. HCMOS circuits would require an average bias of approximately 1.2V for a 5V supply, for example. EDN

Instrumentation amp has low offset, drift, and low-frequency noise

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

Analog Devices' (www.analog.com) digitally gain-programmable AD8231 instrumentation amplifier exhibits zero offset. It has programmable voltage gains, which are successive powers of two, from $2^0=1$ to $2^7=128$ (**references 1** and **2**). The AD825x family also includes some digitally gain-programmable instrumentation amplifiers, which have gain expressed as powers of 10. These amplifiers contain no internal autozero circuitry, however. The composite instrumentation amplifier in **Figure 1** suits applications requiring instrumentation amplifiers having voltage gains of a multiple of 10 and requiring low voltage offset, drift, and low-frequency noise.

The design exploits the fact that the gain is 10^M, where M is an integer, which you can express as $10^M=2^M\times5^M$. The circuit in **Figure 1** employs a cascade of the autozeroed AD8231 instrumentation amp, IC_1, with a preset voltage gain of eight, IC_2, and IC_3. The net result is that the input-voltage offset of IC_2 causes an RTI (referred-to-input) voltage offset, which decreases by a factor of eight compared with an offset of a stand-alone circuit, IC_2. The same holds also for the offset-voltage drift. The auto-zeroing circuitry of the IC_1 decimates the low-frequency noise. EDN

REFERENCES

1 "Zero Drift, Digitally Programmable Instrumentation Amplifier, AD8231," Analog Devices Inc, 2007, www.analog.com/en/prod/0,2877,AD8231,00.html.

2 "10 MHz, 20V/s, G=1, 2, 5, 10 iCMOSR Programmable Gain Instrumentation Amplifier, AD8250," Analog Devices Inc, 2007, www.analog.com/en/prod/0,2877,AD8250,00.html.

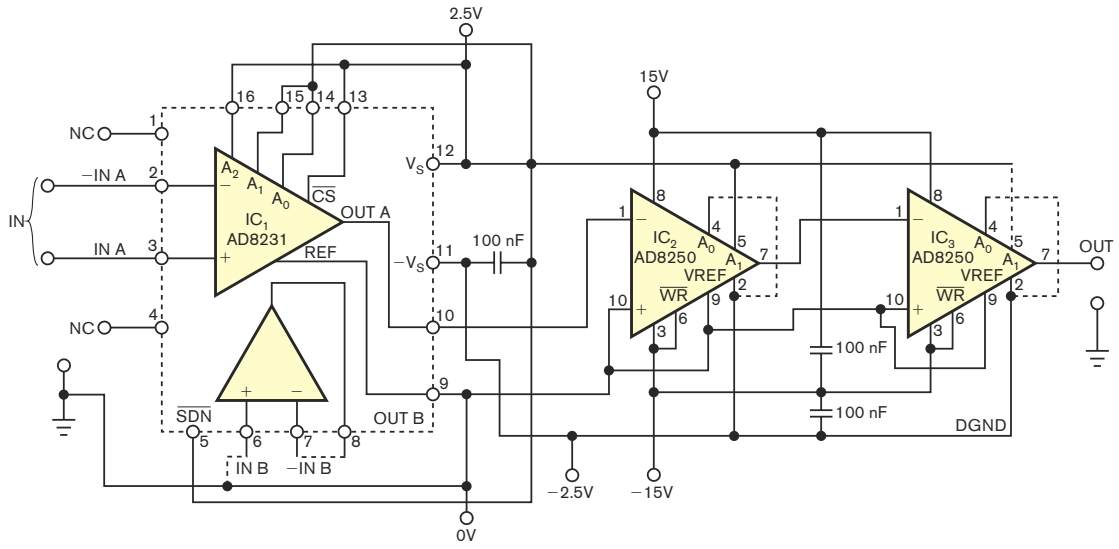

Figure 1 By cascading an autozeroed instrumentation amplifier having a gain of 2^3 and instrumentation amplifiers having gains of five, you get a decade-gain instrumentation amp whose dc performance is much better than that of monolithic decade-gain instrumentation amps.

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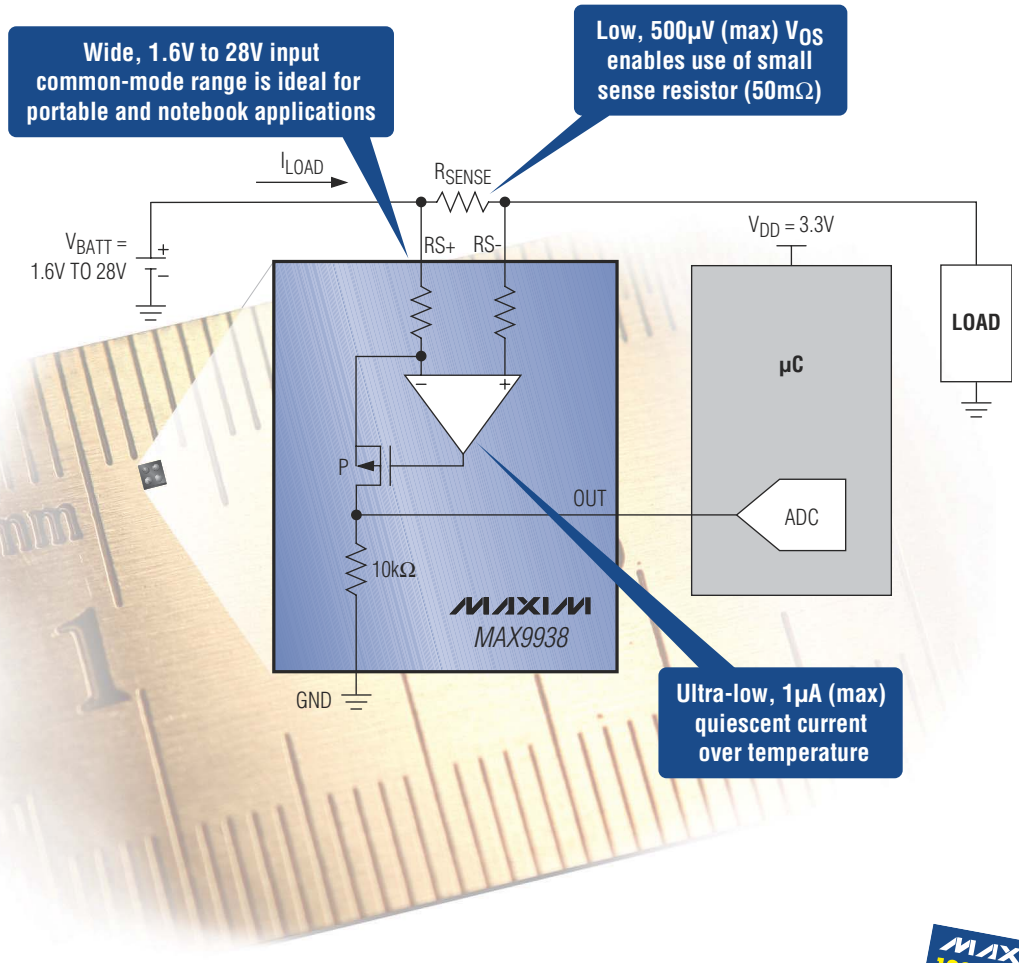

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Four DIPs provide as many as 80 sequential-LED outputs

Greg Carkner, Cobourg, ON, Canada

A previous Design Idea makes clever use of the ability of the 4017 CMOS counters to accept either positive or negative edge-clock signals, even though it leaves two LEDs on at once (**Reference 1**). But what happens if you want more than 19 counts? A quick check in some old CMOS data books uncovered a circuit for using 4017 counters to make sequential displays. However, this approach sacrifices some outputs and yields nine outputs for the first counter and only eight for each subsequent one. It also requires you to add an AND gate between each successive counter stage.

The circuit in **Figure 1** differs from the one in the earlier Design Idea in that it uses HCMOS parts and adds one 74HC540 to facilitate a simple means of multiplexing the outputs of two 4017 counters for as many as 80 outputs. The 74HC540 is a convenient pinout version of the venerable 74HC240-series bus drivers. By including a DIP-resistor network, you can also reduce the discrete-component count for the design. The recommended current-sourcing capability of the HC-series parts at 6V supply is slightly lower than that of the 4000-series parts at 15V, but the reduced resistor losses provide a more energy-efficient circuit if you use better LEDs.

The **figure** omits the necessary supply-bypassing capacitors or a clock or power-on-reset circuit. D_1, D_2, and R_1 form a simple AND gate, which you might use instead of an external reset input to form a continuous ring counter, at which the cathodes connect to selected outputs of each of the counters, IC_1 and IC_2. EDN

REFERENCE

1 Tregre, Jeff, "Cascade two decade counters to obtain 19 sequential outputs," *EDN*, Dec 14, 2007, pg 62, www.edn.com/article/CA6512153.

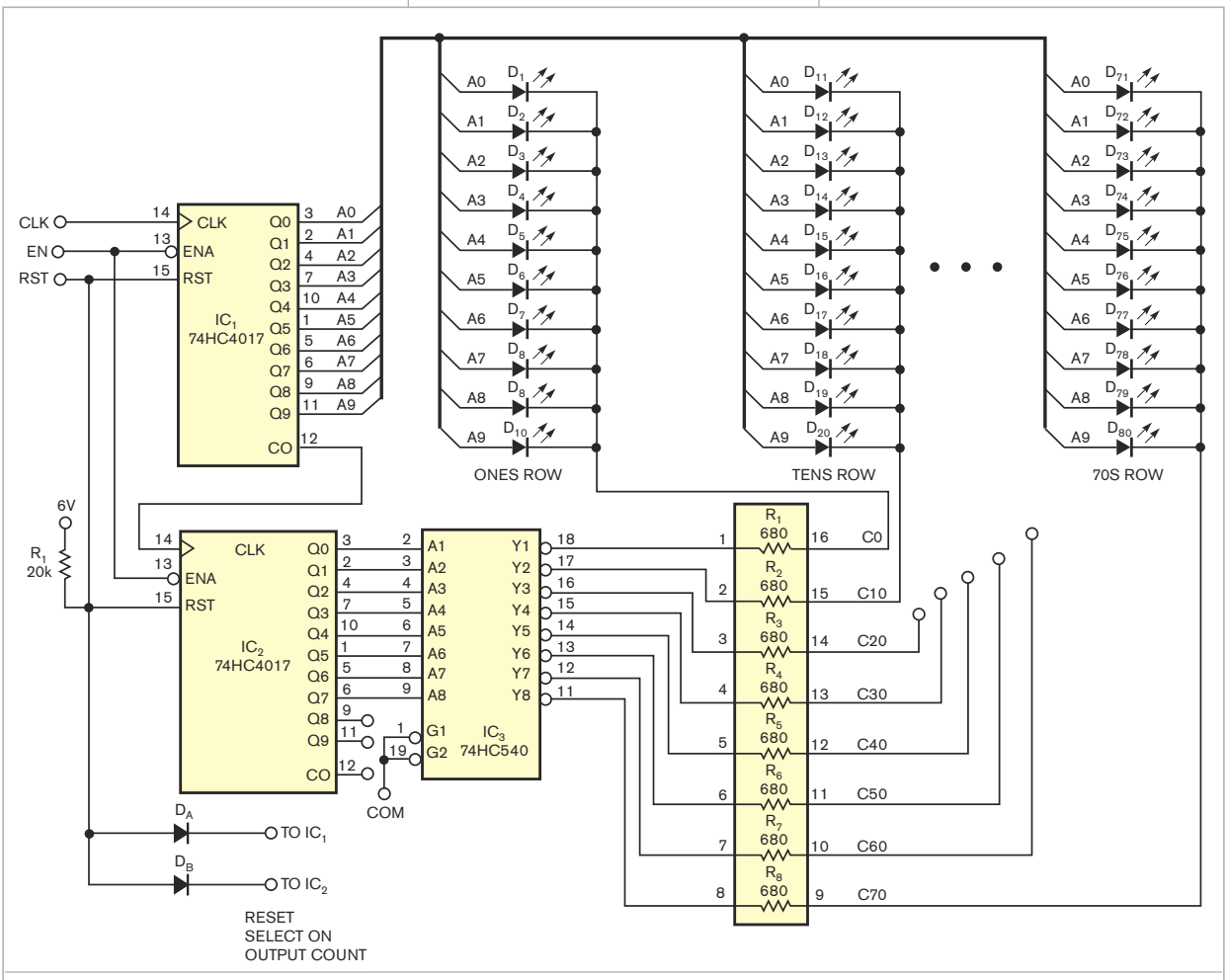


Figure 1 This circuit provides a simple means of multiplexing the outputs of two 4017 counters for as many as 80 outputs.

Program an op-amp gain block with a limited-adjustability, monolithic, solid-state resistor

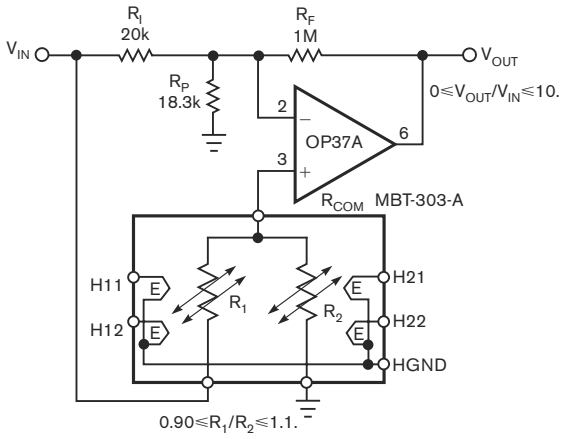
W Stephen Woodward, Chapel Hill, NC

Solid-state replacements for traditional electromechanical trimmer potentiometers are increasingly available in a variety of technologies from a variety of vendors. These replacements have many obvious advantages, such as automatic adjustability, miniaturization, and immunity to vibration. Some of these devices have only limited programmable spans, however. This limitation can sometimes be problematic and may preclude the use of a solid-state option in some design applications. An example of this shortcoming is the Rejustor family of devices, which Microbridge (www.mbridgetech.com) recently introduced. The MBT-303-A Rejustor voltage divider is programmable over a span of only ±10%. When such a limited-capability device sets the gain of a typical amplifier circuit, the correspondingly narrow range of accessible gains may be woefully inadequate.

Figure 1 suggests a generally applicable workaround that works not only with rejustors, but also with all limited-adjustability, programmable dividers with a ±10%-ratio-adjustment range. It uses a single op amp in a differential topology that, in effect, subtracts the minimum programmable-divider ratio from the maximum and amplifies the difference. This approach expands the programmable-gain span to include zero and any desired figure. Potential applications for this trick include any design situation requiring a wide range of inverting and noninverting programmable-gain factors.

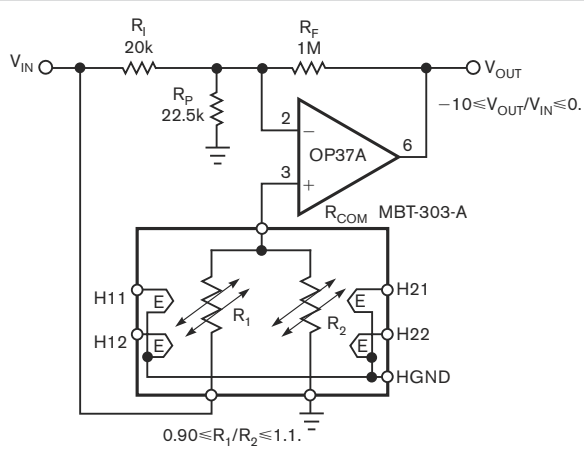
Although the circuit in **Figure 1** implements a programmable gain of zero to 10, you can implement almost any range with a suitable choice of resistors and op amps. **Figure 2** illustrates a gain of zero to −10 for the inverting case. The design equations are R_F/R_I, which is five times the maximum desired gain; $R_P=1/((1/0.9/R_I)-(1/R_F))$ for noninverting gain; and $R_P=1/((1/1.1/R_I)-(1/R_F))$ for inverting gain. The availability of stock resistances sometimes determines a starting value for R_I or R_F. For example, the circuit in **Figure 1**, where R_F has a value of 1 MΩ, accommodates the fact that many inexpensive precision-resistor families, such as those made of metal film, have maximum resistances of 1 MΩ. However, if resistor availability isn't a factor, then choosing R_I to have the same value as R_1 minimizes sensitivity to op-amp bias-current errors. Choosing R_P midway between the resistances for the noninverting- and inverting-gain equations reveals an additional flexibility of the circuit. That variation results in a bipolar—that is, both inverting and noninverting—gain range, with a gain of zero at midspan.

This topology eliminates the inflexibility penalty that limited divider programmability imposes. This benefit, however, incurs a price in the op amp's performance. Because of the partial cancellation of amplifier gain, the gain-bandwidth product and dc accuracy of the op amp must surpass the overall maximum gain and offset requirements of the gain block by at least a factor of five. One way to accommodate this requirement is to incorporate a decompensated, precision op amp, such as the classic OP37, which is stable only for closed-loop gains higher than five. EDN



NOTES:
Set R_P=20.4 kΩ FOR A PROGRAMMABLE-GAIN RANGE OF $-5 \leq GAIN \leq +5$.
$V_{OUT}/V_{IN}=50(R_2/R_1-0.9)=0$ IF $R_2/R_1=0.9$ AND $=10$ IF $R_2/R_1=1.1$.

Figure 1 Adding an op amp and associated components to a Rejustor solid-state resistor allows you to trim the output over the full input-voltage range.



NOTE:
$V_{OUT}/V_{IN}=50(R_2/R_1-1.1)=0$ IF $R_2/R_1=1.1$ AND $=-10$ IF $R_2/R_1=0.9$.

Figure 2 Adjusting the value of R_P allows the circuit to function as an inverting trimmer.

EDITED BY SUZANNE DEFFREE

supplychain

LINKING DESIGN AND RESOURCES

Organic-distributor growth remains steady in unsteady times

In the electronics-distribution industry, merger-and-acquisition activity over the past 20 years has sometimes been as bustling as Grand Central Station during rush hour. A key player in that industry, Digi-Key Corp (www.digikey.com) has managed a healthy 22% compound-annual-growth rate over the last two decades through a solely organic-growth strategy. "We've had plenty of alternatives to capitalize on strategies that would play well into organic growth," says Digi-Key's president, Mark Larson (**photo**), noting the company's volume business division as an example. "We've been able to develop our international business significantly," he continues, providing further example.

"Right now, export sales probably represent more than 30% of our sales. You go back even six or seven years ago, and that [segment] probably would have represented less than 1% of our sales. There have been initiatives that we have been able to implement that have driven the growth that we are comfortable working with without acquisition." Larson, like many other executives across the electronics supply chain, believes that the problem with acquisitions is cultural. "What you anticipate as some kind of synergy may actually never materialize. It's very common in this industry where we've had situations where one plus one equals one and a half," he says.

The organic strategy continues to serve the company well. Despite the harsh economy, Larson in July estimated that 2008 sales were up 8.5% over 2007's $941 million in revenue. "Certainly, the base of this business is still the engineer—the design engineer—and we continue to grow our engineering customer base. … I think, had we been stalled along the way, we might have been more inclined to look at acquisitions, but we've been pretty comfortable with our rate of growth as rated internally," Larson says. "I would never rule out [acquisition as a growth strategy], but I would say, at this point in time, it's not one we are considering."

GREEN UPDATE

IPC BRUSSELS MEETING REVEALS ROHS-REVISIONS CONCERNS

If you worry about the possible changes to the ROHS (restriction-of-hazardous-substances) directive, you are not alone. Industry leaders from across the electronics supply chain came together at an IPC (www.ipc.org) workshop in Brussels this summer to address concerns with the Öko-Institut (www.oeko.de) report on the proposed expansion of ROHS-substance restrictions.

The EU (European Union) Commission contracted Öko-Institut to study the inclusion of additional hazardous substances under ROHS beyond the original six materials: lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyl, and polybrominated diphenyl ether. In its draft report to the commission, Öko recommended the restriction of TBBPA (tetrabromobisphenol A), a flame retardant that protects some 80% of PCBs (printed-circuit boards) and that an EU risk assessment found safe, according to the IPC. In addition to TBBPA, the report suggests bans on HBCDDs (hexabromocylcododecanes), several phthalate plasticizers, and all organic compounds containing chlorine and bromine. "IPC is concerned that Öko-Institut's recommendations are arbitrary and lack a sound scientific basis. Implemented, these recommendations will have a significant negative impact on our members," warns Fern Abrams (**photo**), IPC's director of government relations and environmental policy.

Attendees at the meeting included members of the European Commission and the ROHS Technical Advisory Committee from Brussels and the United Kingdom.

OUTLOOK

CONSUMER TELEMATICS SHIFTS TO IN-CAR CONNECTIVITY

Despite high gas prices and the fact that the automotive industry has hit the skids on the economic downturn in the United States, the consumer-telematics industry continues to see healthy levels of innovation, according to ABI Research (www.abiresearch.com). The research company notes that both BMW and Chrysler plan to bring Internet access or Wi-Fi connectivity to cars in the United States this year. While safety and infotainment remain the cornerstones of consumer-telematics offerings, the current economic climate may shift the focus of many telematics-service providers toward cost-saving applications, such as fuel-consumption monitoring, the company reports.

Meanwhile, ABI Research notes that inflexible, single-application approaches targeting just one automaker could leave some companies on the side of the road. The research company expects versatility to be a major strength of consumer telematics. "Several players are starting to understand that flexible solutions can only be achieved through the adoption of global standards and cooperation among all players in the value chain, with the added incentive of possible cost reductions," says ABI Research Analyst Dominique Bonte.

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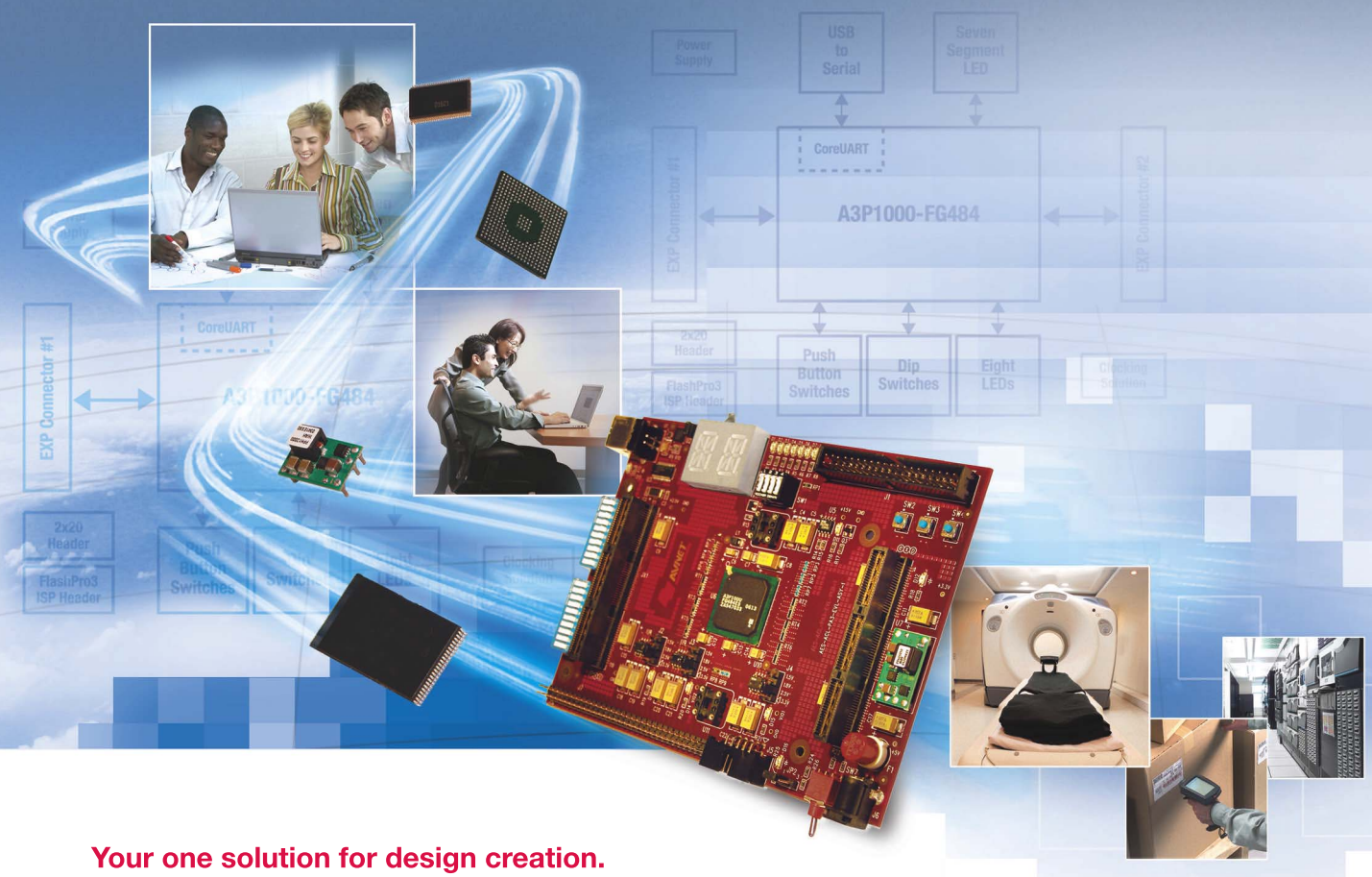

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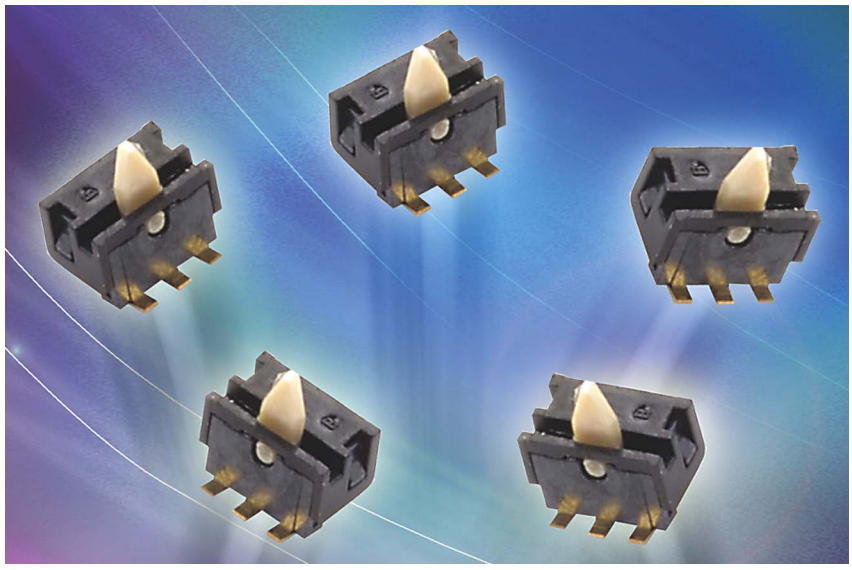
productroundup

SWITCHES AND RELAYS



Pendulum-style detection switch uses top and side actuation

The SDT microminiature surface-mount detection-switch series has a pendulum-style construction, allowing the switch to actuate from the top or the side. The switch provides a 30g-maximum actuation force, and the recommended stroke to actuate the switch is 30° or more off the center line. Additional features include a 1-mA, 5V-dc contact rating; a 1-mΩ-maximum contact resistance; and a 100,000-cycle-minimum mechanical and electrical life. The switches have a −20 to +70°C operating temperature and a −30 to +80°C storage temperature. The devices have a 3.3-mm profile off the PCB and cost $1.50 (12,000).

C&K Components, www.ck-components.com

Hall-effect-IC family includes a variety of switches in small packages

The vendor's Hall-effect-IC-switch family includes unipolar, omnipolar, polarity-discriminating, and bipolar switches. The unipolar switches switch on in the presence of either a south- or a north-pole magnetic field of sufficient strength. Similar to the unipolar switches, the omnipolar switches have separate outputs, switching on after the detection of a north or a south pole. The polarity-discriminating switches provide separate outputs, switching on after the detection of a north or a south pole. The bipolar switches switch on with a south magnetic field of sufficient strength and switch off with a north magnetic field of sufficient strength. Addition features include a 3.5-µA average current, integrated compensation, and push-pull CMOS-logic-output circuitry. Available in a 1.1×1.1×0.5-mm BGA package or a 1.6×1.6×0.6-mm surface-mount package, the unipolar and bipolar Hall-effect ICs cost 11 cents and 64 cents, respectively.

Rohm Electronics, www.rohmelectronics.com

Load switches target high-end, high-current, portable devices

The MIC94040/1/2/3 family of high-side load switches targets high-end, portable, battery-powered consumer devices, including smart-feature phones, personal multimedia and navigation, and ultramobile PCs. Using the vendor's MLF-package technology, the devices feature a 28-mΩ on-resistance and a 3A continuous current. Operating over a 1.7 to 5.5V input, the switches have level-shift circuitry that controls them over 1.5V logic and allows them to control higher-voltage supplies. The MIC94040 and the MIC94041 include a rapid-turn-on option, and the MIC94042 and the MIC94043 provide a slew-rate-controlled soft-start turn-on of 116 µsec, preventing inrush current. The MIC94041 and the MIC94043 provide active-load-discharge circuitry, allowing capacitive loads to automatically discharge when the main switch is off. The MIC94040/1/2/3 devices are available in a 1.2×1.2-mm package, and prices start at 34 cents (10,000).

Micrel, www.micrel.com

Terminal-block relay has plug-in SPDT contacts

Providing plug-in SPDT contacts, the PLC-Relay high-current terminal-block relay aims at applications requiring a 10A nominal-current rating or devices requiring contacts with long electrical life. For shorter installation time, the series uses a patented plug-in-bridging system, requiring no daisy-chain wiring. Suiting use as an alternative to ice-cube relays, the devices connect to 6- to 14-mm PLC-Relays using the press-fit bridge. Measuring 14 mm wide, the PLC-Relay costs $16 (one).

Phoenix Contact, www.phoenixcontact.com

USB/104 I/O solid-state relay-output module provides hot-plug functions

The USB-IDIO-16 USB/104 I/O module has 16 individually optically isolated inputs. The optically isolated inputs include channel-to-channel and channel-to-ground inputs. Compatible with USB 1.1 and 2.0 ports, the module provides hot-plug functions for quick disconnection. The device also provides 16 protected, solid-state-FET, high-side-switch outputs capable of switching from 5 to 34V dc at 2A. The modules are also available in the USB-IDIO-8 eight-I/O version. Available in a 4×4×1.4-mm, rugged industrial enclosure, the USB-IDIO-8 and the USB-IDIO-16 cost $259 and $329, respectively.

Acces I/O, www.accesio.com

RF- and microwave-switch-selection guide is available as a free download

The RF- and microwave-switch-selection guide provides comprehensive information on the vendor's portfolio of switches, primarily comprising electromechanical and solid-state switches. Features include an overview of electromechanical- and solid-state-switch drivers and a switch-driver recommendation based on application needs. The guide also provides characteristic-switch parameters, such as switching speed, isolation, and insertion loss in typical applications and configurations. Selection and option tables provide detailed specifications and options for the vendor's portfolio. A free copy of the RF- and microwave-switch-selection guide is available at the vendor's Web site.

Agilent Technologies, www.agilent.com

EMBEDDED SYSTEMS

MicroTCA carrier hub supports a variety of fabric switches

Targeting the µTCA chassis, the UTC001 MicroTCA carrier hub features a managed mode providing support for GbE, 10-GbE, serial-attached-SCSI, PCIe, and Serial RapidIO switch fabrics. The MicroTCA carrier-management controller manages the power modules, two cooling units, and 12 AdvancedTCA mezzanine cards in the chassis. The basic configuration of the single-piece UTC001 MicroTCA carrier hub costs $1200.

VadaTech, www.vadatech.com

Data-acquisition board eliminates ground loops

The MSXB 084 data-acquisition-processor board includes 16 differential analog inputs. Onboard 16-bit analog-to-digital conversion minimizes the exposure to noise from other circuits in the system. Each board can acquire data at 333k samples/sec. Eight boards in a 19-in., rack-mountable enclosure can connect to a single data-acquisition-processor board. Prices for the MSXB 084 board start at $595.

Microstar Laboratories Inc, www.mstarlabs.com

Rack-mount computer targets space-critical environments

The Relio R4000 rack-mount computer is available with several processor options, including the 500-MHz AMD Geode LX800, 1-GHz UVL Intel Celeron M, or 1.4-GHz Intel Pentium M models. Each system includes dual 10/100BaseT Ethernet, two high-speed USB 2.0 ports, four serial ports, keyboard and mouse ports, and analog video. An internal 100 to 240V-ac power supply powers the R4000. Prices for the AMD LX800 model start at $900, and shipment is from stock.

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BY DAVID R BRYCE • DATARAM CORP

It's an electromagnetic-mechanical world

In the late 1980s, I was working on a currency counter that included an option to detect counterfeit currency. The counter's mechanism consisted of shaft-mounted rollers that transported the bills, one by one, through the machine. A dc motor drove the system, which would guide the bills over a magnetic pickup head where the system would generate different signals depending upon the type of ink the printing process used. In this way, it could detect the ink used on counterfeit currency.

The system applied the weak signal from the magnetic pickup head to a high-gain instrumentation amplifier before some simple analog processing. On some machines, a troublesome noise spike appeared in the signal. We did not correlate the noise with the passage of the currency notes, but its repetition rate varied as we changed the motor speed. In addition, slowing the transport mechanism diminished the amplitude of the noise spike, although the spike never went away, even with the system operating at its lowest speed.

I was tempted to accuse the motor or its control circuitry of injecting the noise, but I had seen quite a bit of motor noise by this time in my career, and it just didn't look the same. In my experience, noise from dc motors tended to resemble broadband noise and was continuous; the noise I was seeing was as spiky as an electrocardiogram.

To rule out the motor, I killed the power supply to the motor-control circuitry. Then, I forced the transport mechanism to move by pulling on a drive belt as fast as I could. The result was significantly slower than the motor could have achieved but fast enough to show that the noise spike was still there. I had vindicated the motor.

By judiciously disconnecting belts and pulleys, I narrowed down the field of search to the rotation of a single shaft and its attached rollers. When I removed the rollers, the noise disappeared; when I replaced the same rollers on the shaft, the noise returned.

I examined the rollers—not much more than aluminum hubs covered with a rubbery surface, neither of which seemed likely to cause electrical noise. I pondered more, idly fingering the Allen wrench I used to loosen the set screws that held the rollers to their shaft. Aha! The set screws! The tiny *steel* set screws had somehow become little magnets, rotating with the shaft only a few inches away from a magnetic pickup head. I had a flashback to my childhood, when my father showed me how moving a magnet near a coil of wire would make an oscilloscope trace jump and wiggle. Same effect; different decade.

I HAD A FLASHBACK TO MY CHILDHOOD, WHEN MY FATHER SHOWED ME HOW MOVING A MAGNET NEAR A COIL OF WIRE WOULD MAKE AN OSCILLOSCOPE TRACE JUMP AND WIGGLE.

I solved the noise-spike problem by changing the set screws to screws made of nonmagnetic stainless steel. Then I went home and called my dad. EDN

David Bryce is a licensed professional engineer in Pennsylvania and currently works at Dataram Corp. He enjoys table tennis and sudoku in his spare time. Like David, you can share your Tales from the Cube and receive $200. Contact edn.editor@reedbusiness.com.

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